20/12

Code No.: R22EC303PC | R22 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Regular) - December- 2024
DIGITAL LOGIC DESIGN
(ECE)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a)	Convert $(378)_{10}$ to octal.	[1M]
b)	Which gates are called universal gates? What are its advantages?	[1M]
c)	Define Min term & Max term.	[1M]
d)	Implement AND gate using NAND gates.	[1M]
e)	Define combinational logic circuit.	[1M]
f)	What is flip-flop?	[1M]
g)	Draw a 3-bit asynchronous down counter.	[1M]
h)	What is meant by state reduction?	[1M]
i)	Write any one difference between Mealy and Moore model.	[1M]
j)	What is meant by finite state machine?	[1M]

PART-B **(50 Marks)**

2.a)	Convert Octal to hexadecimal conversion $(756.603)_8$	[5M]
b)	Encode the data bits 1101 into the 7 bit even parity Hamming Code.	[5M]
	OR	
3.	State De Morgan Theorem and Apply compliment theorem to each of the following expressions. (i) (A + B + C)D (ii) ABC + DEF (iii) AB + CD + EF (iv) XYZ and X + Y + z.	[10M]
4.	Simplify the Boolean expression using K-MAP. $F(A,B,C,D,E)= \Sigma\, m(0,1,4,5,16,17,21,25,29)$	[10M]
	OR	
5.a)	Realization of OR gate using DTL.	[5M]
b)	Realization of AND gate using RTL.	[5M]
6.	Implement the full adder function by using NAND gates.	[10M]
	OR	
7.a)	Compare sequential and combinational circuits.	[5M]
b)	Convert SR- flip-flop into JK-flip-flop.	[5M]
8.	Design and explain the operation of a 4-bit ring counter.	[10M]
	OR	
9.	Design and construct MOD-5 synchronous counter using JK flip flop.	[10M]
10.a)	Explain about FSM in detail with an example.	[5M]
b)	What are the capabilities and limitations of Finite state machines?	[5M]
	OR	
11.a)	Name the elements of ASM chart and define each of them.	[5M]
b)	Explain in detail the ASM technique of designing a sequential circuit.	[5M]

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