

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS

II-B.TECH-I-Semester End Examinations (Supply) - December- 2024
DIGITAL SYSTEM DESIGN
(ECE)

[Time: 3 Hours]

[Max. Marks: 70]

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 20 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A**(20 Marks)**

1. a) Why XS-3 code is called a self-complementing code? [2M]
- b) Write the truth table for $F=(A+B)(C+D)$. [2M]
- c) Define Prime Implicant and Essential Prime Implicant. [2M]
- d) Mention the expressions for difference and borrow of Full Subtractor. [2M]
- e) Define Flip flop. What are the applications of FF. [2M]
- f) Give the comparison between synchronous & Asynchronous counters. [2M]
- g) What is the size of the decoder in 32x4 ROM? [2M]
- h) What are the advantages of PLDs over fixed function ICs? [2M]
- i) Draw CMOS AND gate. [2M]
- j) Define Propagation delay and Fan-out. [2M]

PART-B**(50 Marks)**

2. Convert the following hexadecimal numbers to decimal and binary. [10M]
 (i) B6C7 (ii) 64AC (iii) A492 (iv) 4BAC (v) A0F9.0EB
- OR**
3. How do you convert and design AOI logic in to a (i) NAND logic and (ii) NOR logic. [10M]
 4. Minimize the given Boolean function, $F(A, B, C, D) = \sum m(0, 1, 2, 3, 6, 7, 13, 15)$ using Tabulation method and implement it using basic gates. [10M]
- OR**
5. Design & implement a Full Adder using NAND gates. [10M]
 6. Draw the basic flip flop circuit with NOR gates and Implement D-FF using JK FF with its truth table. [10M]
- OR**
7. Design and implement Mod-10 Synchronous Up counter using T-FFs. [10M]
 8. Differentiate different logic devices. Implement the following Boolean functions using PAL (i) $F1 = AB' + AC + A'BC'$ (ii) $F2 = AC + BC$. [10M]
- OR**
9. Describe the design procedure of synchronous finite state machine (FSM) by taking sequence detector as example. [10M]
 10. Design a 3 input TTL NAND Gate and explain its working. [10M]
- OR**
11. Perform the analysis of standard DTL NAND gate and give its characteristics. [10M]
