Code No.: R22EC57204PE43 | R22 | H.T.No. | | | 8 | R | | | | | |

# CMR ENGINEERING COLLEGE: : HYDERABAD
## UGC AUTONOMOUS
## I–M.TECH–II–Semester End Examinations (Supply) – March 2025
## DESIGN FOR TESTABILITY
## (VLSI SD)

**[Time: 3 Hours]** **[Max. Marks: 60]**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

**PART-A** **(10 Marks)**

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|---|---|---|---|
| 1. | a) | What is the difference between digital and analog VLSI testing? | [1M] |
| | b) | How do trends in VLSI technology impact the testing process? | [1M] |
| | c) | What is the role of true-value simulation in VLSI testing? | [1M] |
| | d) | What is fault simulation, and why is it important in the context of VLSI design? | [1M] |
| | e) | What is the purpose of Digital Design for Testability (DFT) in VLSI. | [1M] |
| | f) | How does Scan Design improve the testability of sequential circuits? | [1M] |
| | g) | Define Random Logic BIST. | [1M] |
| | h) | Why is Memory BIST necessary in VLSI testing? | [1M] |
| | i) | Name one example of a test instruction defined by the Boundary Scan Standard. | [1M] |
| | j) | How does the Boundary Scan Standard ensure compatibility between different devices? | [1M] |

**PART-B** **(50 Marks)**

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|---|---|---|
| 2. | Discuss the role of testing in the design and manufacturing of VLSI circuits. What are the key objectives of testing in VLSI? | [10M] |
| | **OR** | |
| 3. | Explain the different levels of fault models used in VLSI testing. How do gate-level, transistor-level, and physical fault models impact the testing process? | [10M] |
| 4. | Explain the role of simulation in design verification and test evaluation in VLSI circuits. | [10M] |
| | **OR** | |
| 5. | What is Automatic Test Pattern Generation (ATPG), and why is it important for VLSI testing? Discuss the different types of ATPG algorithms and their applications in fault detection. | [10M] |
| 6. | Explain the concept of testability measures in VLSI design. Discuss the significance of controllability and observability in the context of the SCOAP metric. How do these factors impact testability? | [10M] |
| | **OR** | |
| 7. | Describe the variations of Scan Design used in VLSI circuits and how do they impact testability and overall circuit performance? | [10M] |
| 8. | Explain the operation of test per scan BIST systems in VLSI testing. | [10M] |
| | **OR** | |
| 9. | How is pattern generation handled in a Built-In Self-Test (BIST) system? Discuss the methods used to generate test patterns for random logic circuits. | [10M] |

10. Explain the system configuration with Boundary Scan and what are the roles of the TAP controller and port in the configuration? [10M]

**OR**

11. Discuss the importance of pin descriptions in Boundary Scan. How do the pin descriptions help in testing and ensure proper operation of the Boundary Scan system? [10M]

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