Code No.: EC744PE	R20	H.T.No.			8	R						

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
IV–B.TECH–I–Semester End Examinations (Supply) – April - 2025
DIGITAL CMOS IC DESIGN
(ECE)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1.	a)	State the applications of CMOS inverter.	[2M]
	b)	Define rise time and fall time.	[2M]
	c)	What are the advantages of primitives CMOS logic gates?	[2M]
	d)	Define CMOS full adder.	[2M]
	e)	Write a short note on bistable elements.	[2M]
	f)	Write the applications of sequential MOS circuit.	[2M]
	g)	Define dynamic logic circuits.	[2M]
	h)	Explain the advantages of dynamic CMOS transmission gates.	[2M]
	i)	Define memory and its advantages.	[2M]
	j)	What is a DRAM cell?	[2M]

PART-B **(50 Marks)**

2.	With neat sketches, explain the transfer characteristic of a CMOS inverter.	[10M]
	OR	
3.	Define Threshold Voltage. Express dependency of threshold voltage and voltage transfer on various parameters.	[10M]
4.	How the MOS inverters can be designed with NMOS loads. Explain.	[10M]
	OR	
5.	Explain the operation of 3 input CMOS NAND and NOR gates.	[10M]
6.	Draw the logic diagram of a CMOS clocked SR flip-flop and explain with the help of a truth table?	[10M]
	OR	
7.	Describe the operation of edged triggered flip flops.	[10M]
8.	Explain Voltage Boots trapping with an example.	[10M]
	OR	
9.	Discusses about synchronous dynamic pass transistor circuits.	[10M]
10.	Explain the principle of NAND gate flash memory with a neat diagram.	[10M]
	OR	
11.	Compare the SRAM and DRAM.	[10M]

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