CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Supply) - June- 2025
ANALOG & DIGITAL ELECTRONICS
(Common for IT, CSM)

[Time: 3 Hours]   [Max. Marks: 60]

Note: This question paper contains two parts A and B.
   Part A is compulsory which carries 10 marks. Answer all questions in Part A.
   Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A   (10 Marks)

1. a) What is the function of a diode as a rectifier?   [1M]
   b) Define diode switching times.   [1M]
   c) Name the three configurations of a transistor used as an amplifier. [1M]
   d) Define the operating point of a transistor.   [1M]
   e) Classify the difference between CS and CD amplifiers?   [1M]
   f) State one of De Morgan's Laws.   [1M]
   g) What is canonical form?   [1M]
   h) What are logic gates & mention all logic gates?   [1M]
   i) Difference between a latch and a flip-flop.   [1M]
   j) List the applications of a shift register?   [1M]

PART-B   (50 Marks)

2. Demonstrate the V-I characteristics of a diode. Discuss how the characteristics change   [10M]
   with temperature variations and the implications of these changes in practical
   applications.

OR

3. Choose the operation of a diode in clipping and clamping circuits. Provide detailed   [10M]
   diagrams, mathematical analysis.

4. Compare Common Base (CB), Common Emitter (CE), and Common Collector (CC)   [10M]
   configurations.

OR

5. Discuss the concept of the operating point (Q-point) of a BJT. Explain the   [10M]
   significance of biasing in BJT circuits and describe different biasing methods, such as
   fixed bias, voltage-divider bias.

6. Explain the construction, operation, and characteristics of a N- channel Junction Field   [10M]
   Effect Transistor (JFET). Discuss its V-I characteristics.

OR

7. Explain the basic digital operations of a system using logic gates. Discuss the working   [10M]
   principles of OR, AND, NOT, XOR gates. Provide truth tables, logic symbols, and
   Boolean expressions for each gate.

8. Given the Boolean function F(A,B,C,D) represented by the minterms ∑m(1,3,7,11,15), convert it to the Product of Sums (POS) form. Show all steps involved in the conversion, including the identification of maxterms and the construction of the POS expression. [10M]

OR

9. Explain the design and working of a binary adder. Compare the half-adder and full-adder circuits, including their logic diagrams, truth tables, and Boolean expressions. [10M]

10. Design a 4-bit serial-in, parallel-out shift register using D flip-flops. Provide the circuit diagram, truth table for flip-flops. [10M]

OR

11. Design a 3-bit synchronous up-counter using T flip-flops. Provide the state diagram, truth table for flip-flops, and the circuit diagram.. [10M]

****