Code No.: R22EC403ES	R22	H.T.No.			8	R						

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–II–Semester End Examinations (Regular) -June- 2025
ANALOG AND DIGITAL ELECTRONICS
(Common for CSE, CSC)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1.	a)	Define diode reverse saturation current.	[1M]
	b)	Draw the VI diode characteristics.	[1M]
	c)	How do you prevent the thermal runaway?	[1M]
	d)	Write the formula for AC voltage gain in CE amplifier.	[1M]
	e)	Compare voltage gain of CS and CD amplifiers.	[1M]
	f)	Deduce X from $(BA0.C)_{16} = (X)_8$	[1M]
	g)	List the applications of Multiplexers.	[1M]
	h)	What are don't care states?	[1M]
	i)	Write the excitation table for JK flip-flop.	[1M]
	j)	What is meant by state reduction?	[1M]

PART-B **(50 Marks)**

2.		Describe the operation of tunneling phenomenon in tunnel diode. Draw and explain the VI characteristics in the negative resistance region.	[10M]
		OR	
3.		Analyze the circuit for a Full Wave Rectifier. Derive the expression for dc current, dc voltage and rms current.	[10M]
4.	a)	Draw and explain the input and output characteristics of a transistor in CE configuration.	[5M]
	b)	Describe how the Q-point shifts due to temperature variation.	[5M]
		OR	
5.	a)	With suitable diagrams, explain the frequency response of a CE amplifier.	[5M]
	b)	In a two-stage CE amplifier, the gain of the first stage is 50 and the second stage is 40. i) Calculate the overall voltage gain in dB. ii) If the input signal is 10 mV, find the output voltage.	[5M]
6.	a)	Derive the expression for input and output impedance of a CS amplifier.	[5M]
	b)	Compare various logic families.	[5M]
		OR	
7.	a)	(a) In a CD amplifier, the source resistor is 500Ω, and the load resistor is 2kΩ. Given $g_m = 4mS$ (i) Calculate the approximate voltage gain. (ii) Calculate input and output impedance.	[5M]
	b)	Construct the two inputs NOR gate using TTL.	[5M]

8. Obtain the minimum product of sum for the following function [10M]
$f(w,x,y,z) = \bar{x}\ \bar{z} + wyz + \bar{w}\ \bar{y}\ \bar{z} + \bar{x}\ y$ using K-Map.

OR

9. Design a full adder using only universal gates. [10M]

10.a) Develop the circuit of J-K flip flop using NAND gates and explain its operation. [5M]

b) With neat sketch, explain the working principle of Serial in Serial out shift register. [5M]

OR

11. Write a short note on the following memories: [10M]

i) RAM ii) ROM

****