Code No.: AD305PC

R20 H

H.T.No.

CMR ENGINEERING COLLEGE: : HYDERABAD UGC AUTONOMOUS

II-B.TECH-I-Semester End Examinations (Supply) – June - 2025 COMPUTER ORGANIZATION AND MICROPROCESSOR (AI&DS)

[Time: 3 Hours] [Max. Marks: 70]

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 20 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b, c as sub questions.

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	$\underline{PART-A} \tag{20}$	Marks)
1. a)	Define computer organization.	[2M]
b)	What is address sequencing?	[2M]
c)	What are the various registers present in 8086?	[2M]
d)	Which type of operation indicated by status lines of 8086?	[2M]
e)	What is the difference between machine language and assembly language.	[2M]
f)	What is the use of Interrupt service routine?	[2M]
g)	Define Priority interrupt?	[2M]
h)	What is the function of Intel 8089 IOP?	[2M]
i)	What is the need of Cache Memory?	[2M]
j)	Define Arithmetic Pipelining?	[2M]
	<u>PART-B</u> (50 Marks	s)
2.a)	Draw the block diagram of digital computer and explain?	[5M]
b)	Explain design of control unit in detail.	[5M]
	OR	
3.a)	Explain briefly timing and control in basic computer design.	[5M]
b)	Explain micro program example with neat diagram.	[5M]
4.	Draw the architecture of 8086 processor and explain in brief the execution unit and bus interface unit.	[10M]
	OR	
5.	List and explain the instruction set of 8086 with examples.	[10M]
6.	What is an interrupt? Explain about different types of interrupts.	[10M]
	OR	
7.	Explain the Stack Structure Of 8086.	[10M]
8.	Explain Booth Multiplication algorithm with an example.	[10M]
	OR	
9.	Discuss Direct Memory Access (DMA) in detail.	[10M]
10.	With a neat diagram explain about Memory Hierarchy.	[10M]
	OR	
11.	Explain four possible hardware schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching. ***********************************	[10M]