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Code No.: R22EC57101PC | R22 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–I–Semester End Examinations (Regular) - March- 2025
DIGITAL DESIGN & VERIFICATION
(VLSISD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A (10 Marks)

1. a)	What is FIFO?	[1M]
b)	List any two differences between Combinational and Sequential Circuits	[1M]
c)	What is Verilog and why is it used?	[1M]
d)	What are the main applications of VHDL?	[1M]
e)	What are Assertions?	[1M]
f)	What is Perl?	[1M]
g)	Discuss wire load model.	[1M]
h)	What is IR drop?	[1M]
i)	What are Programmable Interconnects?	[1M]
j)	What are the different methods of programming PALs?	[1M]

PART-B **(50 Marks)**

2.	Discuss the different clock distribution techniques used in digital circuits and their trade-offs.	[10M]
	OR	
3.	Explain the function of a barrel shifter and how it differs from a standard shift register.	[10M]
4.a)	Write a Verilog code to implement 3 to 8 decoder.	[5M]
b)	Write a Verilog code to implement 4-bit comparator.	[5M]
	OR	
5.a)	Write a Verilog code to implement D Flipflop.	[5M]
b)	Write a Verilog code to implement Parallel Shift Register.	[5M]
6.a)	What are the characteristics of Perl?	[5M]
b)	What does a Perl identifier mean?	[5M]
	OR	
7.	List the verification guide lines and data types of System Verilog .	[10M]
8.	What are different challenges in PD flow at different steps?	[10M]
	OR	
9.a)	Explain noise and cross talk in SI challenge.	[5M]
b)	Explain the processes of IR drop analysis.	[5M]
10.	Explain the architecture of PLA and programming PLDs.	[10M]
	OR	
11.	Write short notes on PROM, PLA and PAL.	[10M]

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