Code No.: DS305ES	R20	H.T.No.			8	R						

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Supply) – June - 2025
DIGITAL LOGIC DESIGN
(CSD)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Convert the given binary number to octal number $(1010110010)_2 = (\ )_8$.	[2M]
b)	Write the difference between canonical and standard forms with examples.	[2M]
c)	Why are NAND and NOR gates called universal gates?	[2M]
d)	Realize Ex-OR gate using minimum number of NOR gates.	[2M]
e)	Discuss the design procedure of combinational logic circuits.	[2M]
f)	Distinguish decoder and de-multiplexer.	[2M]
g)	Compare combinational and sequential logic circuits.	[2M]
h)	What is of Modulus of a counter?	[2M]
i)	State the types of ROM.	[2M]
j)	List the major differences between PLA and PAL.	[2M]

PART-B **(50 Marks)**

2.	Convert the following numbers from the given base to the other three bases indicated.	[5M]
a)	Binary 11010111 to decimal, octal and hexadecimal.	[5M]
b)	Hexadecimal 2AC5 to decimal, octal and binary.	

OR

3.	Realize all basic logic gates using NAND universal logic gates.	[10M]
4.	Simplify the following Boolean functions using K-maps:	[5M]
a)	$F(A,B,C,D) = \sum(2,3,10,11,12,13,14,15)$.	[5M]
b)	$F(A,B,C,D) = \sum(1,4,5,6,12,14,15)$.	

OR

5.	Minimize the following expressions using K-map. $F(A,B,C,D,E) = \sum(8,9,10,11,12,15,16,18,21,24,25,26,27,30,31)$.	[10M]
6.	Design Half adder and full adder using appropriate truth tables.	[10M]

OR

7.	Implement the function F (A, B, C) = ∑m(2,3,6,7) using a multiplexer and decoder.	[10M]
8.	Illustrate the working of JK flip-flop using NAND gates.	[10M]

OR

9.	Sketch a 3 bit SIPO shift register using D flip-flops.	[10M]
10.	Illustrate the working of PROM, PLA and PAL using a neat diagram.	[10M]

OR

11.	Implement the Boolean expressions F1=XYZ'+XY+YZ and F2=XY'Z+YZ by using Programmable Array Logic device.	[10M]

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