R22EC305ES

Code No.: R22EC305ES

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CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Regular) - December- 2024
DIGITAL LOGIC DESIGN
(DSD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1.	a)	Determine $(377)_{10}$ in Octal and Hexa-decimal equivalent.	[1M]
	b)	State the associative property of Boolean algebra.	[1M]
	c)	Show that a positive logic NAND gate is a negative logic NOR gate and vice versa.	[1M]
	d)	Derive the sum of minterms for the function f(a,b,c)=a′b+b′c′.	[1M]
	e)	Write a short note on priority encoder.	[1M]
	f)	Draw the diagram of 4-Bit Parallel adder.	[1M]
	g)	What is a flip-flop? Write down the characteristic equation of S-R flip flop.	[1M]
	h)	What are shift operations and what are the different types.	[1M]
	i)	List the major differences between PLA and PAL.	[1M]
	j)	Implement half adder in VHDL.	[1M]

PART-B **(50 Marks)**

2.	Explain about even and odd parity check with an example, what is the drawback.	[10M]
	OR	
3.	Implement AND, OR, NOR by using NAND gates only.	[10M]
4.	Obtain the simplified expression in POS of F(w, x, y, z)=π(1,2,4,7,12,14,15) using K-maps.	[10M]
	OR	
5.	Derive and Implement Exclusive OR function involving three variables using only NAND function.	[10M]
6.	Design a combinational circuit with three inputs x,y and z and three outputs A,B and C. When the binary input is 0, 1, 2 or 3 the binary output is one greater than the input. When the binary input is 4, 5, 6 or 7 the binary output is one less than the input.	[10M]
	OR	
7.	What are Magnitude comparators? Explain the design of magnitude comparators with the help of a suitable example.	[10M]
8.	A sequential circuit with two D flip flops A and B, input X and output Y is specified by by the following next state and output equations A (t+1)= AX+BX, B(t+1)= A`X, Y= (A+B) X`. Draw the logic diagram and derive state table and state diagram.	[10M]
	OR	
9.	Design a MOD 5 Synchronous counter using JK flip flops.	[10M]
10.	A combinational circuit is defined by the functions: F1= $\sum m$ (3, 5, 7) F2=$\sum m$ (4,5,7) Implement the circuit with a PLA having 3 inputs, 3 product terms and two outputs.	[10M]
	OR	
11.	Write data flow description of a half adder in VHDL. Draw the truth table and derive the Boolean expressions, simulate and verify the circuit.	[10M]

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