Code No.: R22EC303PC | **R22** | **H.T.No.** | | | **8** | **R** | | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B. TECH–I–Semester End Examinations (Supply) - June- 2025
DIGITAL LOGIC DESIGN
(ECE)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1.	a)	Write a short note on weighted binary codes?	[1M]
	b)	State and prove De morgan theorems.	[1M]
	c)	Implement OR gate using NAND gates only.	[1M]
	d)	Define Pair Quad and Octet in K-maps and give examples for each.	[1M]
	e)	What is the difference between Decoder and Demultiplexer?	[1M]
	f)	Draw the logic circuit of a Half adder and give its truth table .	[1M]
	g)	Define a Register.	[1M]
	h)	Write a short note on Parity bit generator.	[1M]
	i)	What are Mealy and Moore models?	[1M]
	j)	What are the advantages of ASM chart?	[1M]

PART-B **(50 Marks)**

2.	What is a Hamming code and Encode data bits 0101 into a 7-bit Even parity Hamming code.	[10M]
	OR	
3.	Explain various number systems and codes and their conversion with examples for each.	[10M]
4.	Minimize the following expression using K-map and realize using NAND gates $F(A,B,C,D)= \sum m(1,3,7,11,15)+ \sum d(0,2,5)$.	[10M]
	OR	
5.	Discuss about RTL logic family in detail, with one example.	[10M]
6.	Explain about a NOR gate Latch in detail, with a neat diagram.	[10M]
	OR	
7.	Realize a Full subtractor using Decoders.	[10M]
8.	Design a 3-bit synchronous counter with T-Flipflop and draw the diagram.	[10M]
	OR	
9.	Explain the operation of Synchronous and Asynchronous counter.	[10M]
10.	What are the capabilities and limitations of Finite state machines? Explain.	[10M]
	OR	
11.	Explain in detail about State Equivalence and Machine minimization.	[10M]

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