Code No.: R22EC57202PC | R22 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Supply) – March 2025
LOW POWER VLSI DESIGN
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a)	Differentiate between static and dynamic power dissipation.	[1M]
b)	List the different low-power design methodologies.	[1M]
c)	How do high-capacitance nodes impact power dissipation?	[1M]
d)	Describe the use of clock gating to minimize power consumption.	[1M]
e)	Explain about the impact of logic synthesis on power consumption.	[1M]
f)	What is the role of multipliers in low-power arithmetic operations?	[1M]
g)	Explain about the use of cache memory and its power optimization.	[1M]
h)	Describe the importance of SRAM over DRAM.	[1M]
i)	Define the low-power clocking techniques.	[1M]
j)	Define low power clocking in microprocessors.	[1M]

PART-B **(50 Marks)**

2.	Discuss the effects of supply voltage (Vdd) and threshold voltage (Vt) on circuit speed and power consumption.	[10M]
	OR	
3.	Describe transistor sizing, gate oxide thickness and their impact on power optimization.	[10M]
4.	Discuss the high-performance approaches in power minimization	[10M]
	OR	
5.	Explain briefly about	
a)	Energy recovery.	[5M]
b)	Reversible pipelines.	[5M]
6.a)	Explain briefly about the power minimize techniques.	[6M]
b)	Write the advantages and disadvantages of MTCMOS technique.	[4M]
	OR	
7.	Design and explain the operation of CMOS multiplier for low power consumption.	[10M]
8.a)	Describe different methods used to reduce leakage power in memory circuits.	[5M]
b)	Compare and contrast between SRAM and DRAM.	[5M]
	OR	
9.	Discuss low power SRAM technologies with neat diagrams.	[10M]
10.	Discuss the implementation challenges faced in low-power microprocessor design.	[10M]
	OR	
11.a)	How does instruction scheduling affect power consumption in processors?	[5M]
b)	Discuss the importance of low-power clocking in microprocessor design.	[5M]

****