Code No.: R22EC57203PE32 | R22 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Supply) – March 2025
SOC DESIGN
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a) Write the characteristics of CISC. [1M]
   b) Does RISC Architectures simple or complex? [1M]
   c) What are the advantages of NISC? [1M]
   d) What are the main challenges in power optimization in SOC design? [1M]
   e) Why gate level simulation is required? [1M]
   f) How to improve the gate level performance? [1M]
   g) What is clock gating? [1M]
   h) What is Dynamic clock frequency and voltage scaling? [1M]
   i) What is the role of trail paths in SOC? [1M]
   j) Why the verification is important in SOC design? [1M]

PART-B **(50 Marks)**

2. Discuss SOC Architectural issues. [10M]

OR

3. Differentiate elaborately RISC and NISC features. [10M]

4. Explain the ADL for design and verification of ASIP. [10M]

OR

5. Explain NISC design flow and Architecture. [10M]

6. Explain simulation models. [10M]

OR

7. Differentiate data path and control path. [10M]

8. Analyze voltage scaling for low power SOC. [10M]

OR

9. Discuss DCFS techniques. [10M]

10. Describe graph theory for synthesis constructs. [10M]

OR

11. Explain technology independent synthesis. [10M]

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