Code No.: R22EC603PC

R22	H.T.No.			8	R					

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
III–B.TECH–II–Semester End Examinations (Regular) - June- 2025
VLSI DESIGN
(ECE)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a)	Mention remedies for latch-up effect.	[1M]
b)	Define self-aligning process in transistor fabrication.	[1M]
c)	How do you contact polysilicon with diffusion?	[1M]
d)	Mention λ-based design rules.	[1M]
e)	Sketch the circuit diagram of transmission gate.	[1M]
f)	Mention the advantages of dynamic gates.	[1M]
g)	Compare SRAM and DRAM.	[1M]
h)	What is meant by Zero/One detector?	[1M]
i)	Define Standard Cells.	[1M]
j)	Write the Principle of Testing inVLSI.	[1M]

PART-B **(50 Marks)**

2.a)	Explain why I_D becomes independent of V_{DS} (I_{DS}Vs V_{DS}) saturation.	[5M]
b)	The MOS transistor having V_{gs} =2.5V, V_t =0.5V, V_{ds} =2.5V and $\mu_n C_{ox} W/L$ =100μA/V^2 . Find the I_{ds} and determine the transistor operating region.	[5M]
	OR	
3.a)	Determine the pull-up and pull-down ratio (Z_{pu}/Z_{pd}) for an NMOS inverter driven by another nMOS inverter.	[5M]
b)	Explain clearly about different operating regions in CMOS inverter with neat diagrams.	[5M]
4.	With relevant examples discuss the estimation of capacitance for the following (i) Sigle layer (ii) Multiple layers.	[10M]
	OR	
5.	Design a layout diagram for the following function in CMOS logic. $F = \overline{AB + C + D}$	[10M]
6.	How switch logic can be implemented using Pass Transistors and explain with an example.	[10M]
	OR	
7.	Implement the following function using dynamic CMOS logic. $F = \overline{AB + C(D + E)}$	[10M]
8.	Design an Arithmetic and Logic unit circuit with four functions by using full adder logic (Ripple Carry Adder).	[10M]
	OR	
9.a)	Examine the working principle of Booth's Multiplier with suitable example.	[5M]
b)	Describe the working operation of 1T DRAM cell.	[5M]

10.a) Compare CPLDs and FPGAs. [5M]

b) Demonstrate the test principles with suitable examples. [5M]

OR

11.a) Implement the following functions using PAL [5M]

$$F_1(A,B,C,D) = \sum_m (0,2,3,4,6,8,9,10,11,13,15)$$

$$F_2(A,B,C,D) = \sum_m (0,1,2,4,6,8,10,11,13,15) + d(3,5,7,14)$$

b) List out all the possible struck at faults for three input NAND gate. [5M]

****