Code No.: IT301ES	R20	H.T.No.			8	R						

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Supply) - December- 2025
ANALOG & DIGITAL ELECTRONICS
(Common to IT, CSM & AI&DS)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Draw the V-I characteristics of diode.	[2M]
b)	What is Bias? What is the need for biasing?	[2M]
c)	Write the characteristic of CE amplifier.	[2M]
d)	What are the types of distortion in amplifiers?	[2M]
e)	Write the expression for basic current equation in MOSFET.	[2M]
f)	Define CMRR and SLEW rate.	[2M]
g)	What is Gray code?	[2M]
h)	What is minterm?	[2M]
i)	What are the basic types of shift registers?	[2M]
j)	Compare asynchronous and synchronous counters.	[2M]

PART-B **(50 Marks)**

2.	How the reverse saturation current of a diode does varies with temperature? Explain.	[10M]
	OR	
3.	Explain negative peak clipper with and without reference voltage.	[10M]
4.	Prove that the transistor acts as an amplifier with suitable circuit diagram.	[10M]
	OR	
5.	Derive the expression for A_{VS}, A_{IS}, R_i, R_o of transistor amplifier using CB configuration	[10M]
6.	Explain the operation and characteristics of N- channel JFET	[10M]
	OR	
7.	Explain about 2 inputs CMOS NAND Gate.	[10M]
8.	Draw the schematic diagram and truth table for full adder. Explain the design approach for full adder using universal gates. Draw the relevant logic diagrams with necessary expressions	[10M]
	OR	
9.	What is a half-adder? Design a half adder using NAND – NAND logic gates.	[10M]
10.	Discuss about synchronous and ripple counters.	[10M]
	OR	
11.	Explain the operation of clocked SR flip-flop with its truth table.	[10M]

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