Code NO: R22EC403ES common for CSE, CSC

Analog & Digital Electronics II B.Tech II Sem (Supply) Dec-25

PART-A

1(a) Static Resistance:-

Ratio of DC voltage to DC current at a point on V-I characteristics

$$R = \frac{V}{I}$$

Dynamic Resistance:-

Ratio of small change in voltage to small change in current.

b) A rectifier is an electronic circuit that converts AC into DC

c) operating point is the steady DC voltage and current at which a device operates when no input signal is applied.

d) Thermal Runaway is a condition in which an increase in temperature causes an increase in current, which further increase temperature, leading to device failure.

e) FET:- It is a voltage controlled semiconductor device in which current is controlled by an electric field.

f) Demorgan's Law:-

1. $(A+B)' = A'B'$
2. $(AB)' = A'+B'$

g) Minterm and Maxterm:-

Minterm: A product (AND) of all variables where the output is 1

Maxterm:- A Sum (OR) of all variables where the output is zero

h) Don't care conditions:- are input combinations for which the output is not specified and can be treated as either '0' or 1 to simplify logic circuits

i) Flip Flop:- It is a bistable multivibrator used to store one bit of binary data

j) Shift Register:- It is a group of flip flops used to store and shift data left or right on each clock pulse.

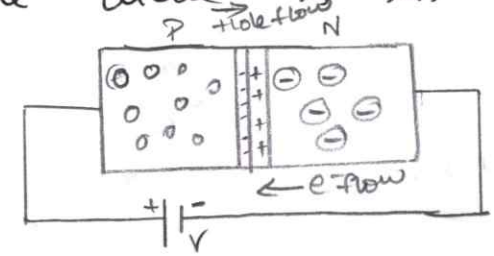
PART-B

2. A P-N Junction diode is a two terminal semiconductor device formed by joining P-type and N-type materials. It allows current to flow only in one direction.

Operation of P-N junction diode:-

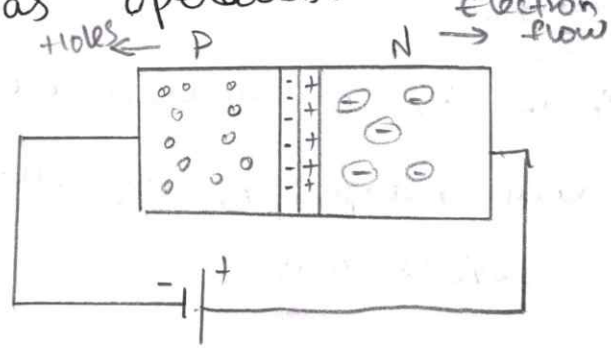
Forward Bias operation

when positive terminal is connected to p-side and negative terminal is connected in n-side than the diode is in Forward bias.



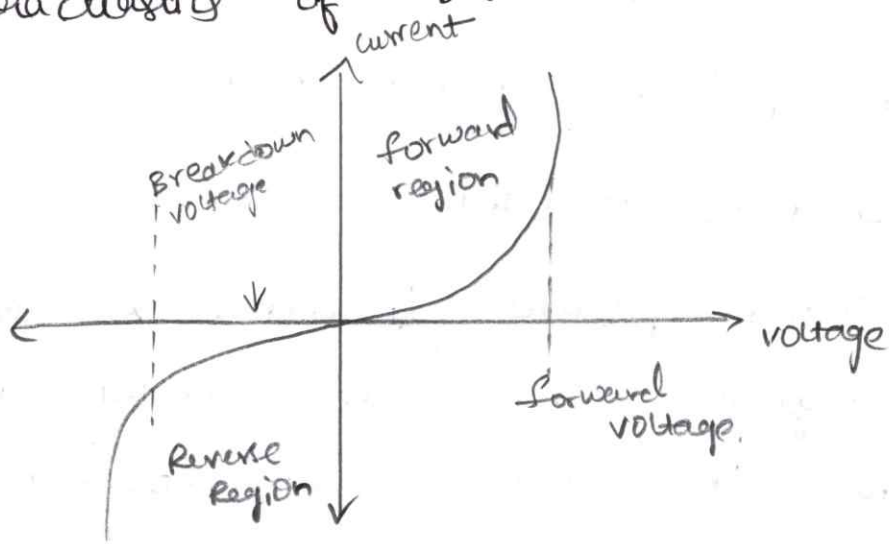
External voltage reduces the depletion layer width
Barrier potential decreases.
Large current flows with small increase in voltage

Reverse Bias operation:-



when positive terminal is connected to -ve terminal and -ve terminal is connected to P- side. than the diode is known as Reverse Bias.

V-I characteristics of Diode.



Forward characteristics :-

x axis voltage

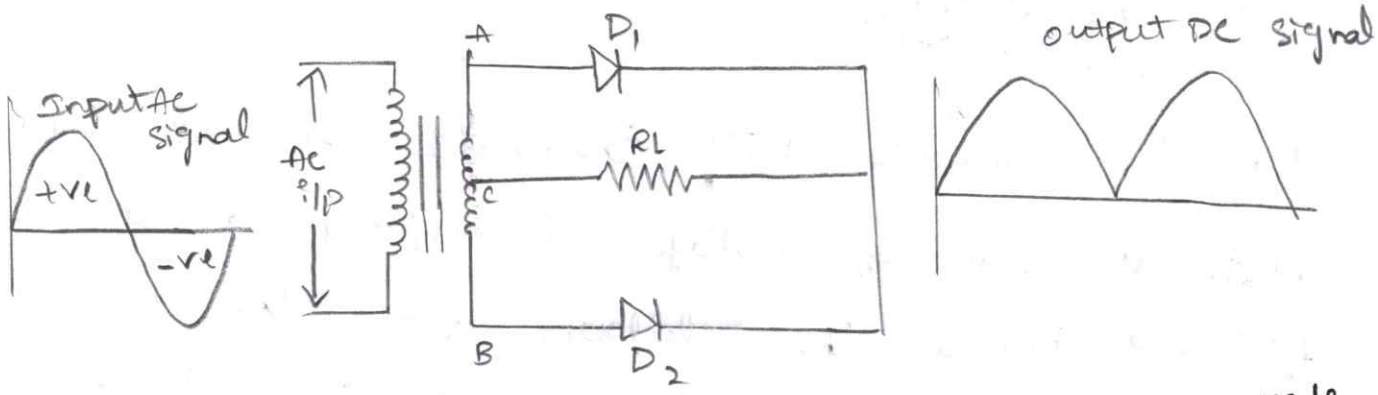
y axis current

Diode conducts in forward bias. After cut in voltage there will be a rapid increase in current

Reverse characteristics :-

There is a sudden rise in current at breakdown voltage blocks current in reverse bias.

3.



Full wave Rectifier is a component which converts A.C into DC. During positive half cycle of the ac Input signal passes through the circuit. D_1 is in Forward bias & D_2 is in Reverse bias D_1 conducts and current flows the voltage across R_L in direction

During -ve half cycle D_1 is in Reverse Bias and D_2 is in Forward bias, D_2 conducts and current flows in the voltage across R_L

Ripple Factor

$$\Gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} = 0.48$$

Efficiency

$$\eta = 81.2\%$$

$$V_{dc} = (2 * V_m)\,\pi$$

$$I_{rms} = V_{RMS} / R_L$$

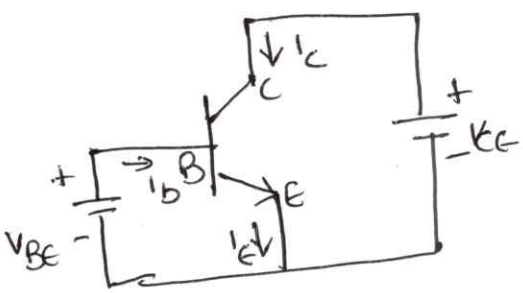
$$I_{Lmax} =$$

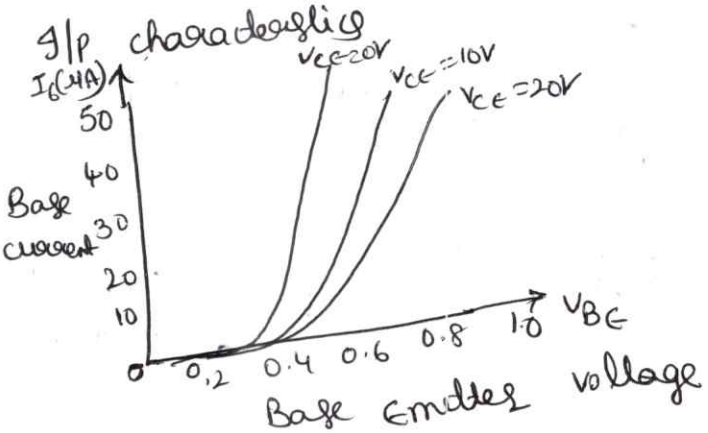
$$V_{rms} = \frac{V_{max}}{\sqrt{2}}$$

4 CE configuration

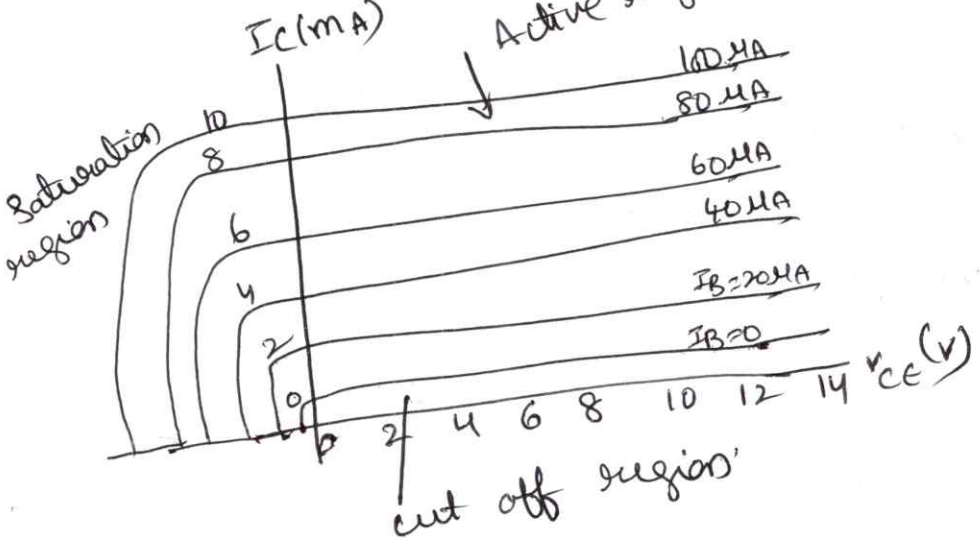
Let us consider NPN transistor in CB configuration when the emitter voltage is applied as it is forward biased the electrons from the -ve terminal repel the emitter electrons and current flow through the emitter and base to the collector to contribute collector current. The collector Voltage V_{CB} is kept constant

In collector current is much larger than that of base current. So the current gain in CE configuration is very large



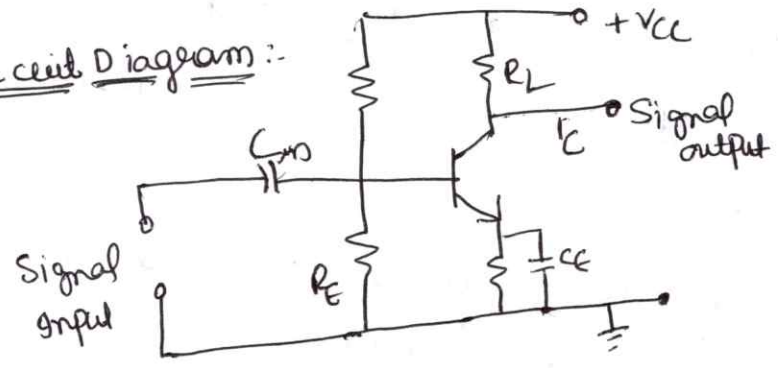


O/P characteristics



5 Single stage RC coupled amplifier

Circuit Diagram :-



A single stage RC coupled amplifier is CE configuration that uses Resistor capacitor network to process and couple signals. It is widely used for pre amplification of weak audio signals due to its simple design and wide frequency.

Working :- A weak AC signal is applied to the base of the transistor through the input capacitor C_{in} small variation in the collector current due to transistor gain.

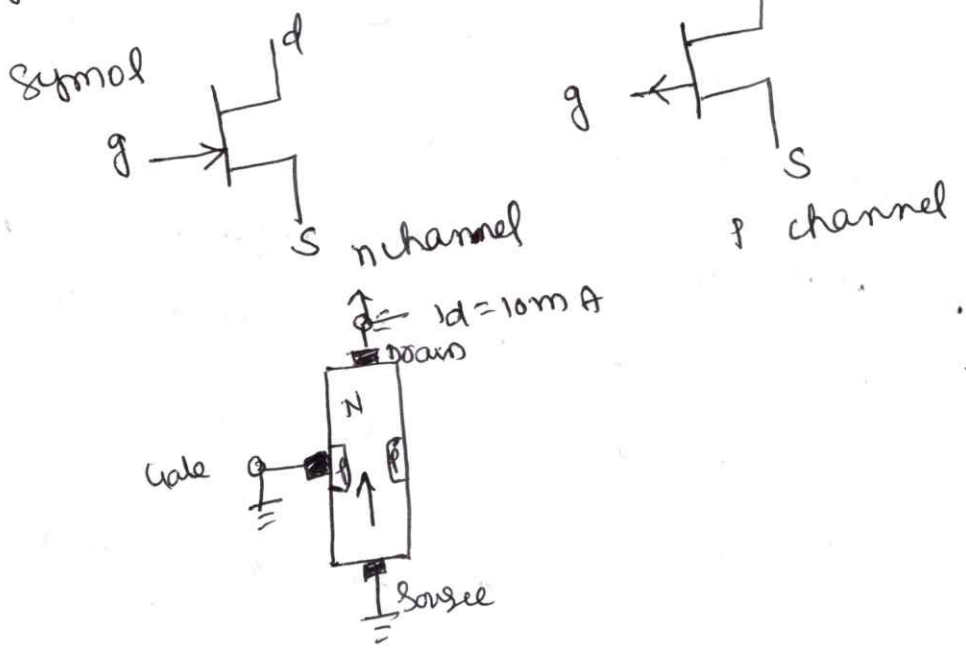
The output signal is taken at the collector 180° out of phase with the i/p signal.

The amplified AC signal is coupled to the output terminal via C_C which filters out any DC bias voltage

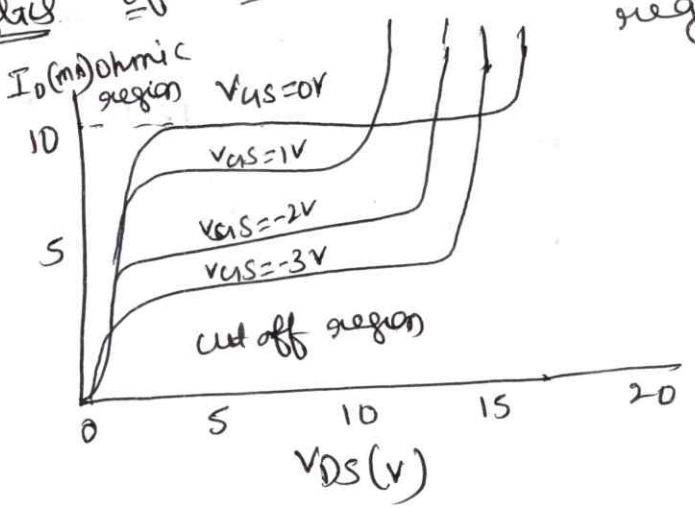
6 JFET:-

It is a voltage controlled device. the current carried only one type so it is a unipolar device no minority charge carries.

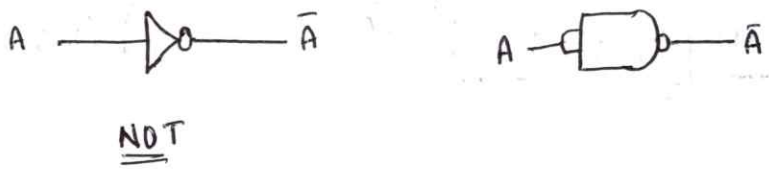
The reverse biased gate junction produced a depletion layer in the region of the channel the gate volt controls the thickness of the depletion layer and hence the thickness of the channel



Characteristics of JFET

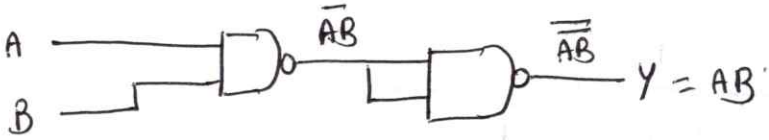


7. Logic Gates using NAND Gates.

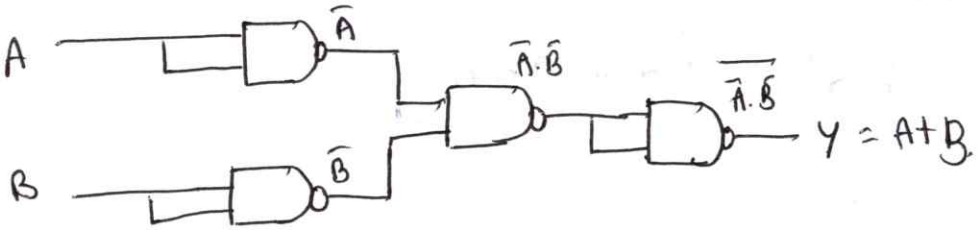


NOT

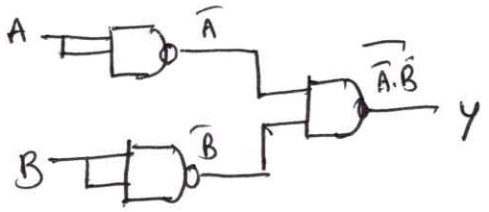
AND using NAND



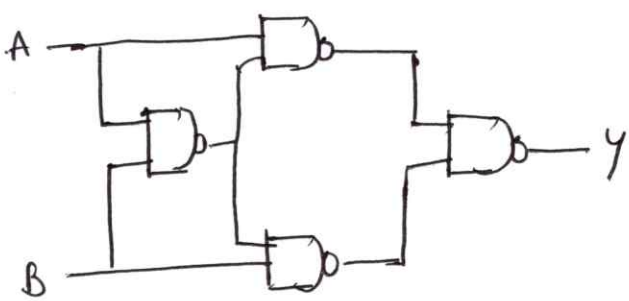
NOR using NAND



OR using NAND

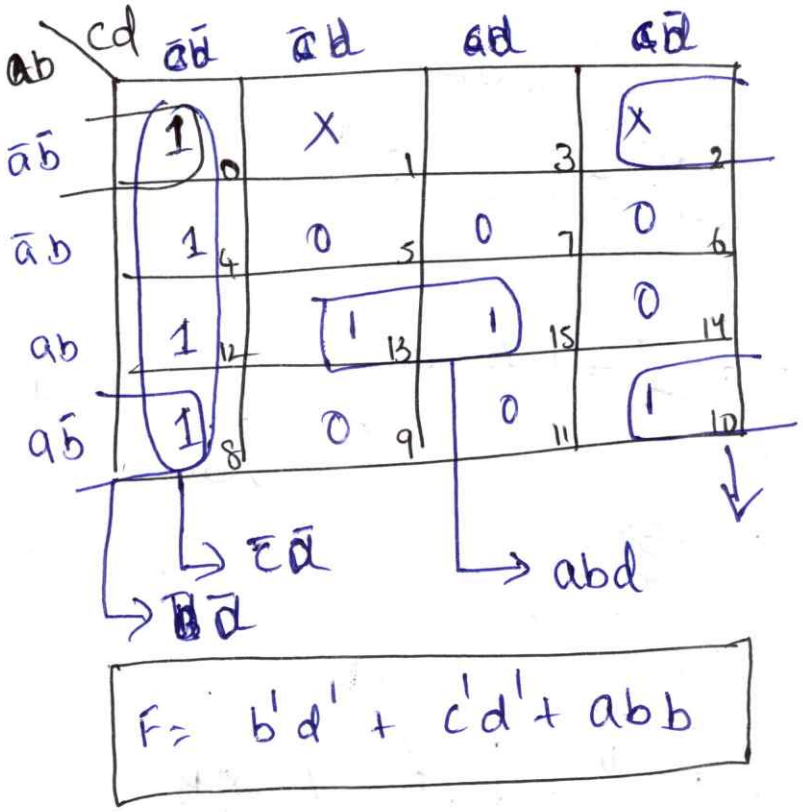


XOR using NAND



8 k - map

$F(a, b, c, d) = \Sigma m(0, 4, 8, 10, 12, 13, 15) + d(1, 2)$

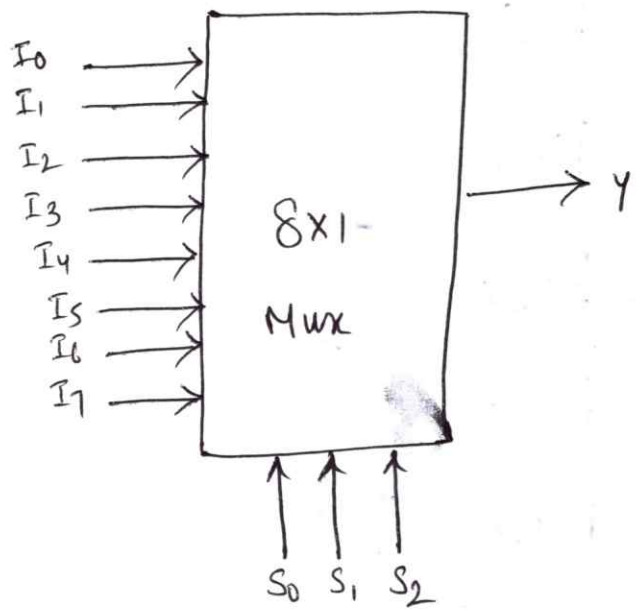


$F = b'd' + c'd' + abb$

9. 8x1 Multiplexer:-

A Multiplexer is also known as Mux. It is a combinational logic circuit that is designed to accept multiple input signals and transfers only one of them through the output line.

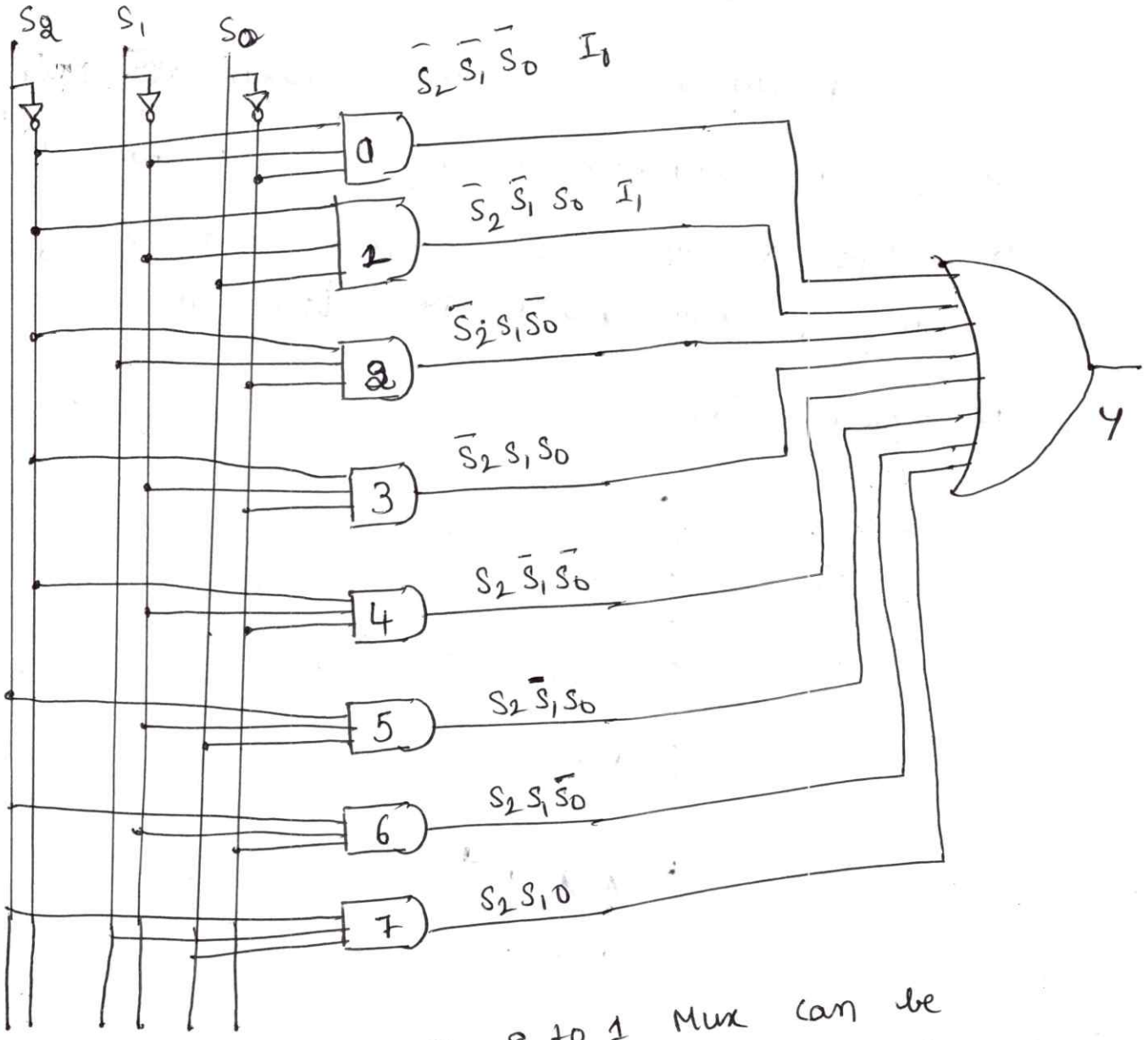
The block Diagram:-



Truth Table:-

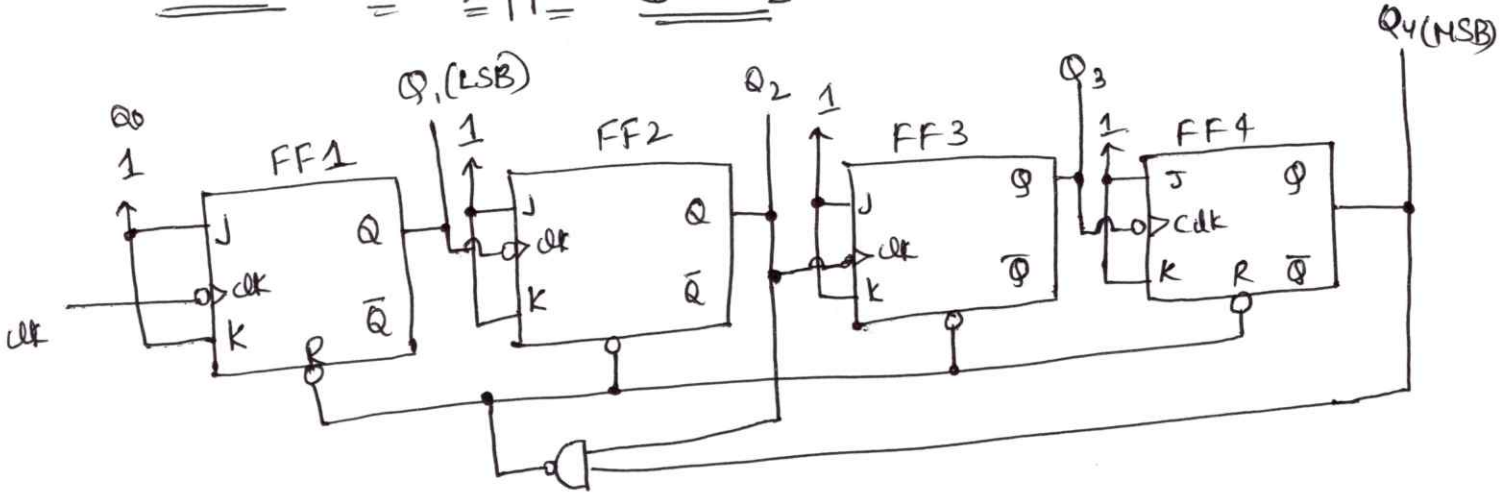
S_2	S_1	S_0	Y_0
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

Logic Diagram

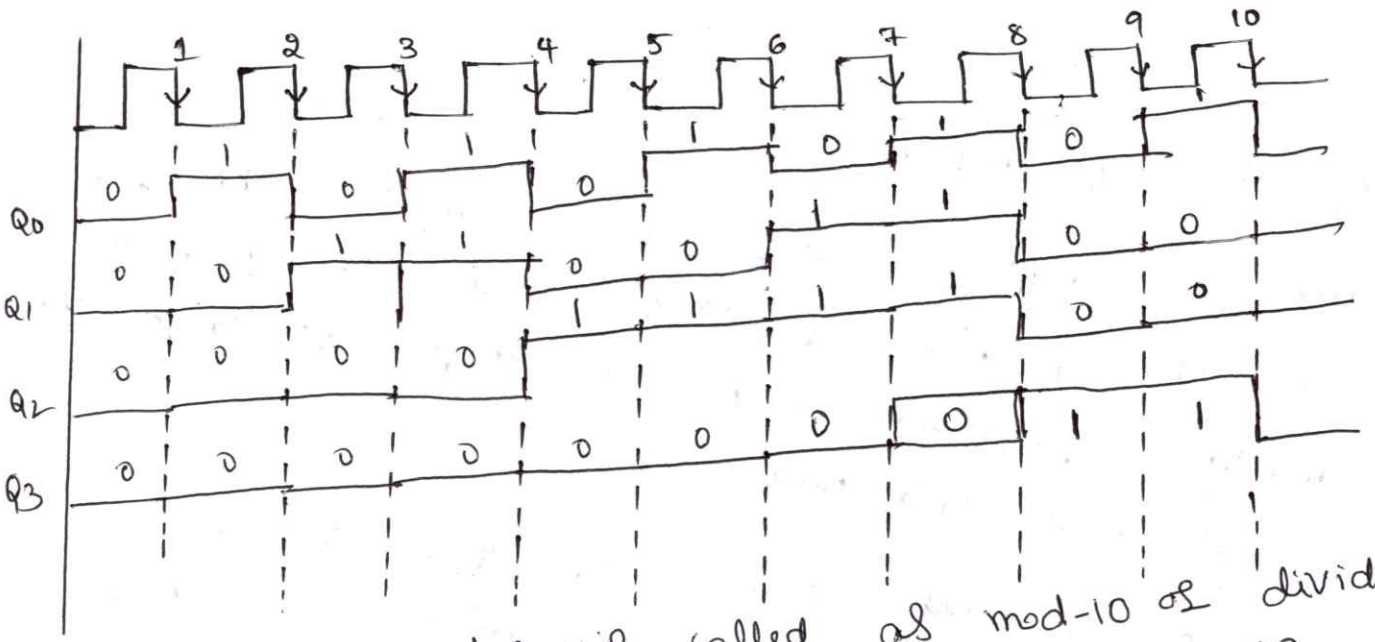


In the logic diagram 8 to 1 Mux can be implemented by using 8 AND gates, 1 OR gate and 3 NOT gates The output gate connected to only one of the n data inputs at a given instant of time. The output is selected based on the truth table of this Integrated circuit.

10. Modulo 10 ripple counter



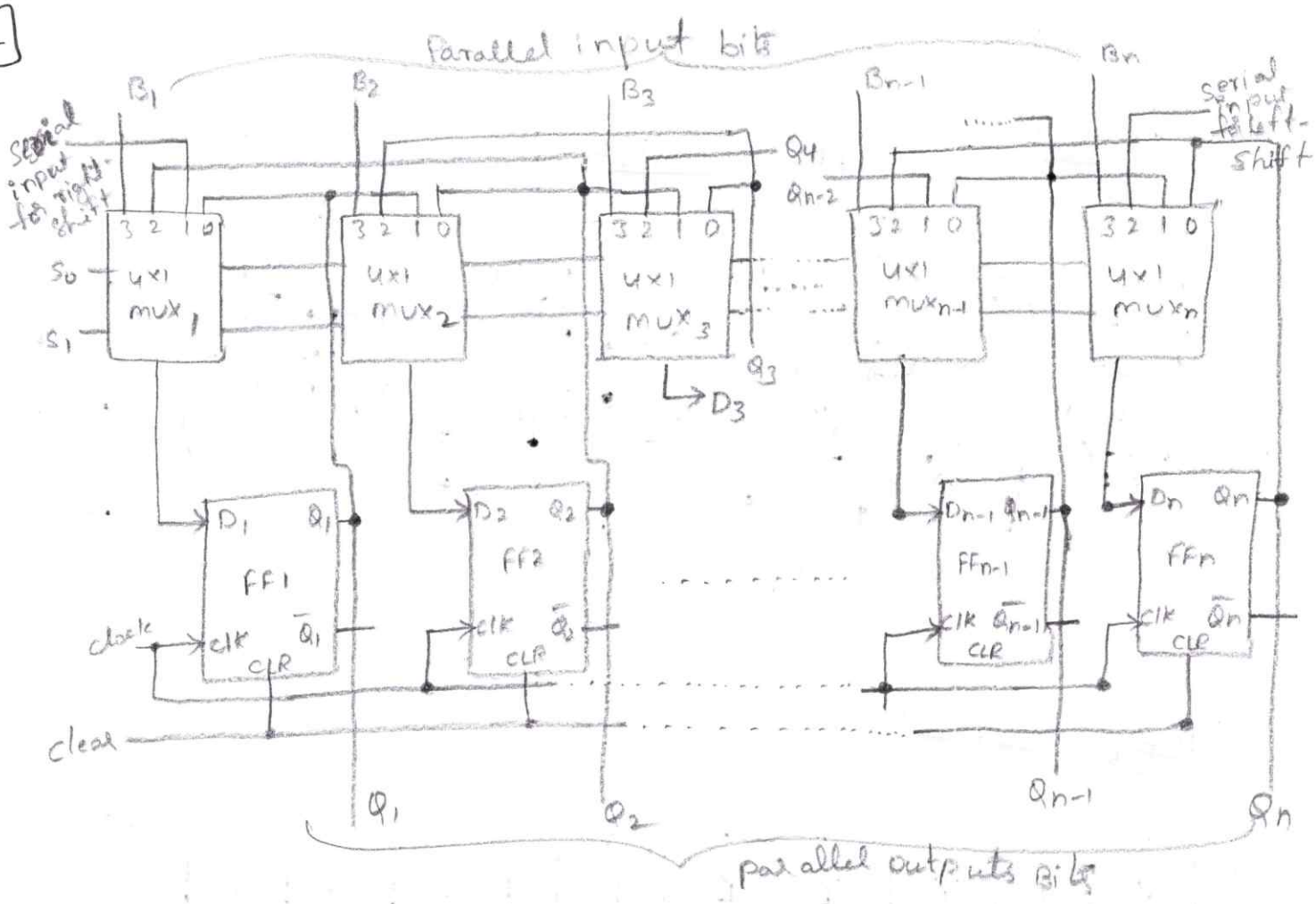
Timing Diagram:-



A decade counter is called as mod-10 or divide by 10 counter. It counts from 0 to 9 and again reset to 0. It counts in natural binary sequence

Mod-10 counter using JKFF counts from 0 to 9 (10 states) and resets

11]



Universal Shift Register

4 bit universal shift register is a digital ckt that can store 4 bits of data and can perform multiple operations such as shift left, shift right parallel load and hold.

It is ~~connected~~ consists of four flip flops connected in cascade with multiplexers at their inputs. The multiplexers select the required operation based on control inputs S_1 and S_0

S_1	S_0	operation
0	0	Hold
0	1	shift right
1	0	shift left
1	1	parallel load.

Scheme of Evaluation :-

PART-A

1. a) Define Static and Dynamic — 1 mark

b) What is rectifier — 1 mark

c) Definition — 1 mark

d) Definition — 1 mark

e) Definition — 1 mark

f) Definition — 1 mark

g) Definition — 1 mark

h) Definition — 1 Mark

i) Definition — 1 mark

j) Definition — 1 Mark

PART-B

2. Working of PN junction Diode → 5 marks
   V-I characteristics → 5 marks

3. Working of Full wave Rectifier → 5 marks
   Expression for RF, Efficiency, V_{dc}, I_{rms} → 5 marks
   I_{Lmax} & V_{rms}

4. circuit Diagram → 2 Marks
Explaination → 3 Marks
output characteristics → 5 Marks

5 circuit Diagram → 2 Marks
Explaination → 5 Marks
o/p Diagram → 2 Marks

6 principle of operation → 5 Marks
V-I characteristics → 5 Marks

7 All logic Gates
Each Gate → 2 Marks
2×5 = 10 Marks

8 K-Map → 8 Marks
Expression → 2 Marks

9 Logic Diagram → 4 Marks
Truth Table → 4 Marks
Block Diagram → 2 Marks

10 Block Diagram → 4 Marks
working → 3 Marks
Timing Diagram → 3 Marks

11 Diagram → 4 Marks
working → 6 Marks.