Code No.: CS403ES	R20	H.T.No.			8	R					

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–II–Semester End Examinations (Supply) - December- 2025
ANALOG & DIGITAL ELECTRONICS
(Common to CSE, CSC)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1.	a)	What is a PN diode and how does it work?	[2M]
	b)	What are the advantages of using a full-wave rectifier over a half-wave rectifier?	[2M]
	c)	What are the different regions of operation in a transistor?	[2M]
	d)	Explain the thermal runaway.	[2M]
	e)	What are the differences between BJT and FET?	[2M]
	f)	Explain the De-Morgans laws.	[2M]
	g)	Explain the Exclusive-OR gate properties.	[2M]
	h)	How does a 2-to-4 decoder work and what is its truth table?	[2M]
	i)	Compare between latch and flipflop.	[2M]
	j)	What is the need of state reduction in sequential circuits?	[2M]

PART-B **(50 Marks)**

2.	How do you calculate the current through a PN diode in forward bias?	[10M]
	OR	
3.	What is the peak inverse voltage (PIV) rating of the diodes used in a full-wave rectifier, and how is it determined? How does the load resistance affect the output voltage and current of a full-wave rectifier?	[10M]
4.	Explain the concept of "Common Emitter" configuration and its current-voltage characteristics.	[10M]
	OR	
5.	Explain the CE amplifier and gain bandwidth product.	[10M]
6.	What is the pinch-off voltage in a FET, and how does it relate to the FET's operation as an amplifier?	[10M]
	OR	
7.	Explain the Low frequency Common Source (CS) amplifier.	[10M]
8.	Simplify function using K-Map method for f (A, B, C) =$\sum$ (0, 3, 7) +d (1,5) and implement logic circuit using NAND gates.	[10M]
	OR	
9.	Explain the magnitude comparator and draw a logic diagram.	[10M]
10.	Design a mod 5 synchronous counter.	[10M]
	OR	
11.	Draw a JK flip flop logic diagram and characteristic equation. What are the disadvantages of JK Flip Flop?	[10M]

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