# * SCHEME OF EVALUTION *

## (Analog & Digital Electronics

### PART-A (10 marks)

| | | marks |
|---|---|---|
| (1) a | Correct forward & reverse char with knee point | 1 |
| b | Convert AC to DC | 1 |
| c | Increase amplitude of the signal | 1 |
| d | Q - point for linear operation | 1 |
| e | $V_{GS} > V_T$ | 1 |
| f | cmos Diagram | 1 |
| g | NAND & NOR | 1 |
| h | Any valid TWO applications | 1 |
| i | Any two differences | 1 |
| j | EPROM/EEPROM | 1 |

(2) a) Diode current Eq$^n$ — (3) m
Apply boltzmann relation - 1m
final expression Justification - 1 m

(2) b) Saturation current formula — 3 m
substitution & simplification — 2 m

(3) full wave rectifier + Ripple factor
ckt diagram — 3m
operation — 2m
Expression for Eq$^n$ — 2 m
Ripple factor — 3 m

(4) small sgl diagram — 3 m
Derivation — 3 m
overall gain — 3m
Loading Effect - 1m

5 (a) Dc load line — 2m
Ac load line — 2m
Q-point — 1m

5 (b) fixed bias — 2m
self bias — 2m
Stability exp — 1m

(6) Small signal model diagram — 3m
gm, rd derivation — 4m
Hybrid-π model — 3m

7 (a) Logic gates
for gate diagrams — 3m
for True table — 2m

7 (b) cmos gate diagram + operation — 5m
True table - 3m, operation — 2m

(8) POS & SOP exp.
True Table — 3m
min SOP — 4m
max POS — 3m

(9) 2-bit comparator
T.T — 3m
Boolen Expression — 3m
Logic diagram — 4m

(10) J-K F.F
Logic symbol — 3m, T.T — 2m, characterstic Eqn — 3m
Excitation Table — 2m

(11) Asynchronous up/down
counter diagram — J-K FF — 4m
Timing diagram — 3m
up/down control — 3m

KEY PAPER

CMR Engineering college

(UGC Autonomous)

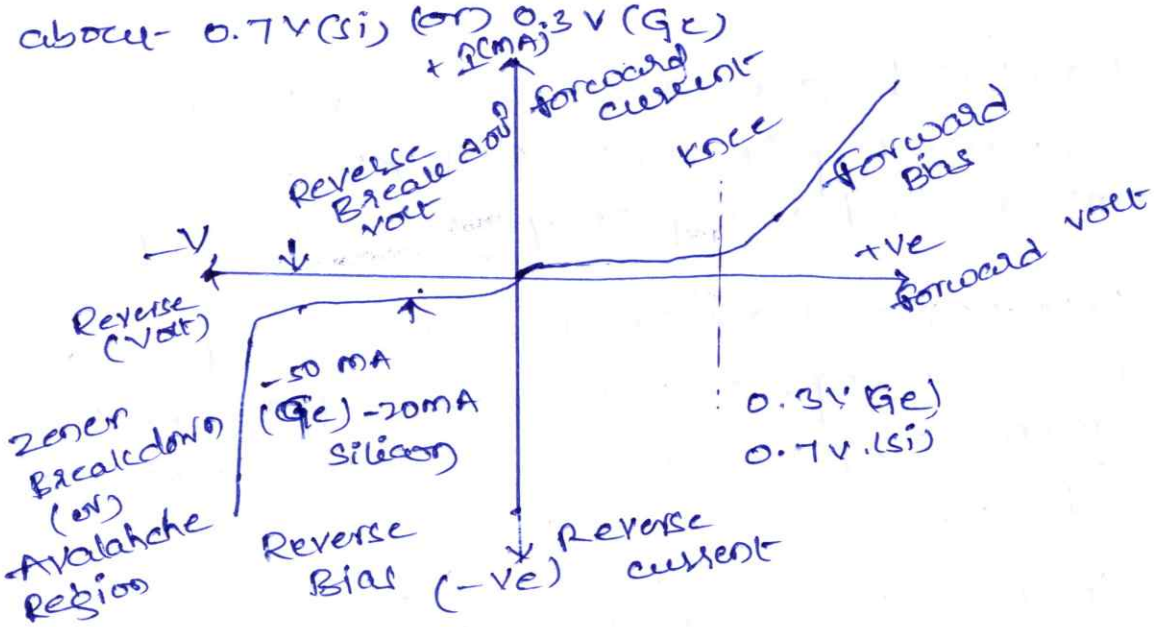
II B.Tech I-Sem End Exam (Reg) - Dec - 2025

ANALOG & DIGITAL ELECTRONICS

PART - A

(1) A) Draw V-I characteristics of a p-N junction Diode?

Ans: A P-N junction diode conducts very small current in reverse bias, and in forward bias. exponetial rise in current after the cut-in (Knee) voltage of about 0.7V(Si) (or) 0.3V(Ge)



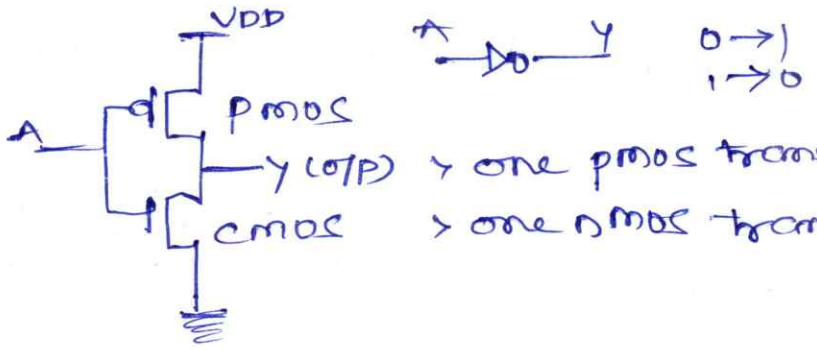

B) Because it converts AC to DC, 'rectifying'

C) Amplifier is a electronic device(or) circuit that increase the amplitude of a weak signal without changing the shape.

D) Biasing is needed to set the transistor's operating point (Q-point) so that it amplifies signal without distortion.

e) Threshold voltage ($V_{th}$) is the minimum Gate-to-Source voltage required to create a conducting channel between drain & source.

f) cmos logic circuit




> one pmos transistor connected to VDD
> one nmos transistor connected to ground.

g) Universal Gates are NAND & NOR, because any logic families (AND, OR, NOT, XOR etc.) can be implemented using only NAND (or) only NOR

h) Applications of mux are used in data routing, communication systems, function generation, parallel-to-serial conversion, and ALU design.

i) Shift register :- shifts data left/right : used for data storage & transfer.
Ripple counter :- counts pulses in binary : used for frequency division and timing.

j) Programable memories are memory devices whose contents can be written (or) programmed by the user, such as PROM, EPROM, EEPROM & Flash.

2) A) When P-N junction diode is forward biased by a voltage V. the minority-carrier concentrations at the edges of the depletion region increase according to Boltzmann relation

$p_n(0) = p_{n0} e^{qV/kT}$, $n_p(0) = n_{p0} e^{qV/kT}$

the excess minority carriers injected are

$\Delta p_n(0) = p_{n0}(e^{qV/kT} - 1)$ $\Delta n_p(0) = n_{p0}(e^{qV/kT} - 1)$

the diffusion current densities at the edges of the depletion regions are

$J_p = qV \frac{D_p}{L_p} \Delta p_n(0)$, $J_n = q \frac{D_n}{L_n} \Delta n_p(0)$

Total current density $J = J_n + J_p = qV \left( \frac{D_n}{L_n} n_{p0} + \frac{D_p}{L_p} p_{n0} \right) (e^{qV/kT} - 1)$

let the term in brackets be the saturation current density $J_s$

$I = AJ = I_s (e^{qV/kT} - 1)$

$I_s = Aq \left( \frac{D_n}{L_n} n_{p0} + \frac{D_p}{L_p} p_{n0} \right)$

final diode current (shockley) Eqn

$$I = I_s (e^{qV/kT} - 1)$$

B) $T_1 = 300K$, $T_2 = 400K$, $I_{s1} = 7.5 \mu A$

$I_s(T) = I_s(T_1) \frac{T_2}{T_1} \exp - \frac{E_g}{K} \left( \frac{1}{T_2} - \frac{1}{T_1} \right)$

$E_g = 1.12 eV$

$K = 8.617 \times 10^{-5} eV/K$.

Temp ratio: $\frac{T_2}{T_1}^3 = \frac{400}{300}^3 = (1.333)^3 = 2.37$

exponential term: $\frac{1}{T_2} - \frac{1}{T_1} = \frac{1}{400} - \frac{1}{300} \Rightarrow 0.0025 - 0.00333$

$= -0.00083$

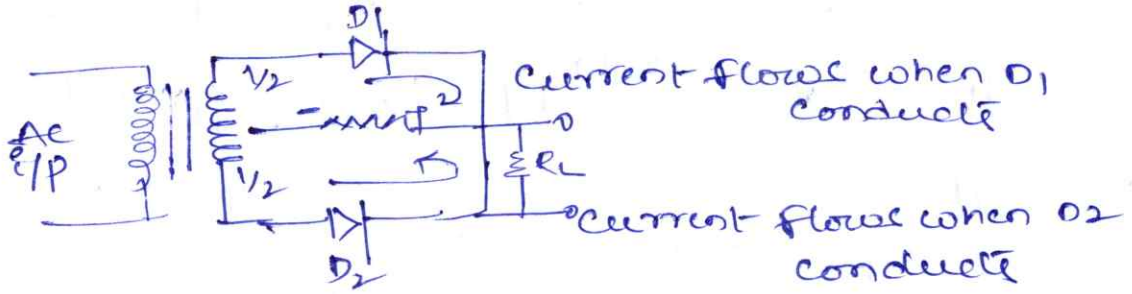
$\frac{E_g}{K} = \frac{1.12}{8.617 \times 10^{-5}} = 12998 \Rightarrow \approx 4.8 \times 10^4$

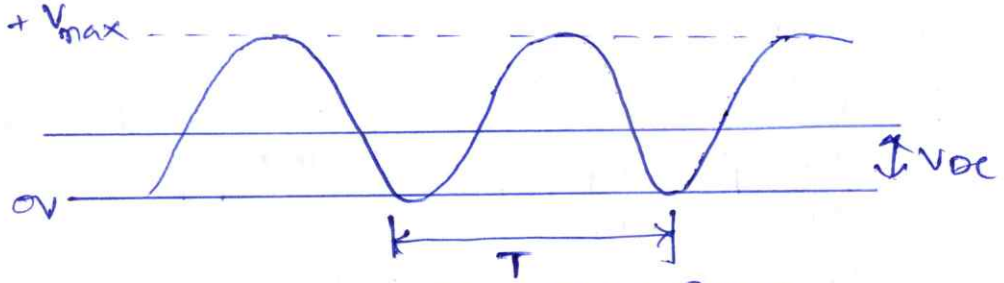
new saturation current

$(I_{S2}) = 7.5 \times 10^{-6} \times 2.37 \times 4.8 \times 10^{4}$

$I_S(400K) \approx 0.86\ A$

3 full wave rectifier.




o/p wave form.

→ Wave form behaviour with capacitor filter — (1) m

$$\Delta t = \frac{1}{2f}$$

⇒ Derive the ripple factor — (4m)

→ Capacitor discharge b/w peaks

$$\Delta t = \frac{1}{2f} \Rightarrow \Delta V = V_{pk} - V_{min} \approx \frac{I_L \Delta t}{C} = \frac{I_L}{C} \cdot \frac{1}{2f}$$

$$V_{r(pp)} = \Delta V = \frac{I_L}{2fC}$$

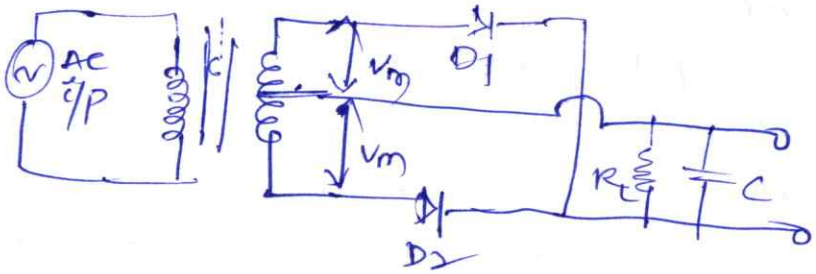
⇒ Rms value of ripple $\Rightarrow V_{r(rms)} = \frac{\Delta V}{2\sqrt{3}}$

Sub $\Delta V$:

$$V_{r(rms)} = \frac{I_L}{4\sqrt{3} f C}$$

⇒ ripple factor $= r = \frac{V_{r(rms)}}{V_{DC}} \Rightarrow \frac{1}{4\sqrt{3} f R_L C}$

full-wave center-tapped rectifier with capacitor




∴ Describe the o/p.

**Q** Multistage Amp:- The transistor circuit which involves more than one stage (or) multi stages of amplification is called a multistage amp.


i.e $A = A_1 \times A_2 \times A_3 \cdots \times A_n$

$$A = \frac{V_{o1}}{V_{in1}} \times \frac{V_{o2}}{V_{in2}} \times \cdots \times \frac{V_{on}}{V_{inn}}$$

* Voltage gain ($A_V$) = $\frac{\text{o/p volt}}{\text{i/p volt}}$.

Stage 1:- $A_{V_1} = \frac{\text{o/p volt of the first stage}}{\text{i/p volt of the first stage}}$

$$A_{V_1} = \frac{V_2}{V_1}$$

Stage 2:- $A_{V_2} = \frac{\text{o/p volt of the } 2^{nd} \text{ stage}}{\text{i/p volt of the } 2^{nd} \text{ stage}} = \frac{V_3}{V_2}$

$$A_V = \frac{V_2}{V_1} \times \frac{V_3}{V_2} \times \frac{V_4}{V_3} \times \cdots \frac{V_n}{V_{n-1}}$$

$$\boxed{A_V = A_{V_1} \times A_{V_2}}$$

∴ Can also be determined by using the relation

$$\boxed{A_V = \frac{A_I R_{C_2}}{R_{i_1}}}$$

5 A) The DC load line represents all possible combinations of transistor collector current $I_C$ and collector-emitter voltage $V_{CE}$ when only DC voltage is resistive load

$$V_{CE} = V_{CC} - I_C R_C$$

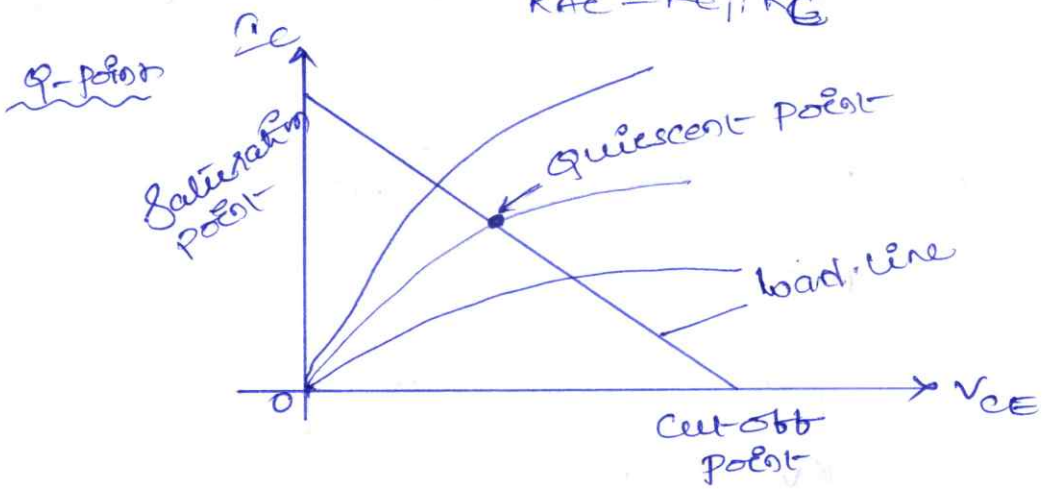
Where $V_{CC}$ → Cut-off point

$V_{CC}/R_C$ → Saturation point

The AC load line is the transistor behaviour for AC signal

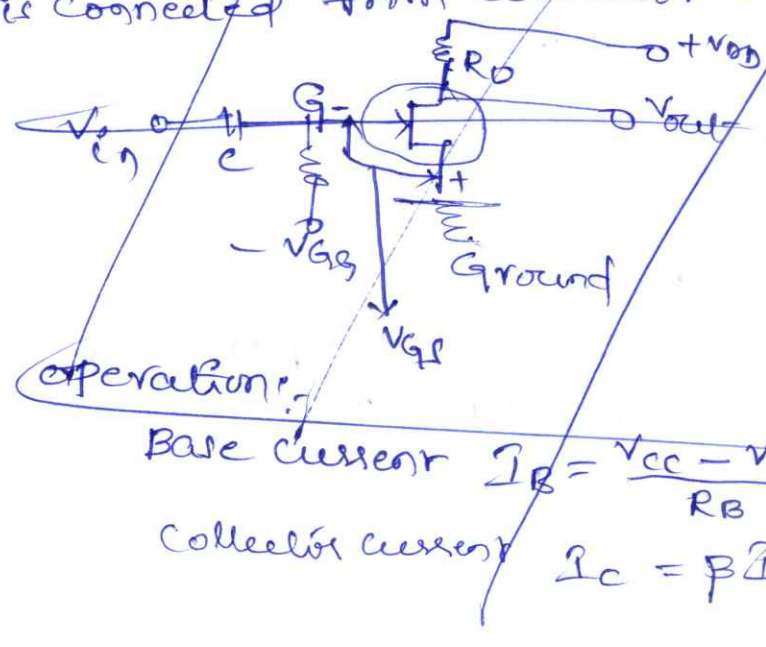
→ $R_C$ in parallel with load resistor

$$R_{AC} = R_C \,||\, R_L$$




5 B) fixed & self Bias circuit

Fixed bias circuit: A resistor $R_B$ connects base directly to supply $V_{CC}$ Another resistor $R_C$ is connected from collector to $V_{CC}$



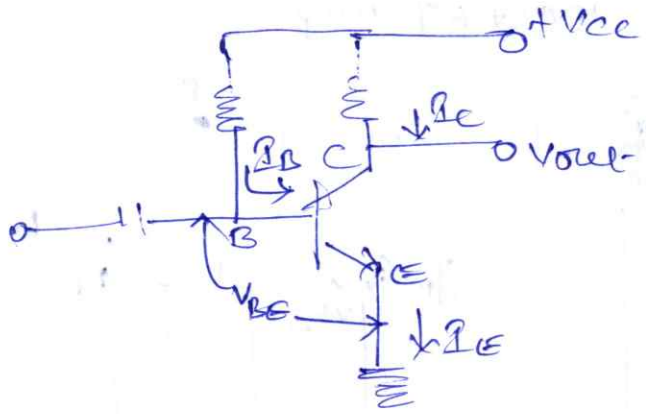

operation:

Base current $I_B = \frac{V_{CC} - V_{BE}}{R_B}$

Collector current $I_C = \beta I_B$

5 B

fixed bias circuit:

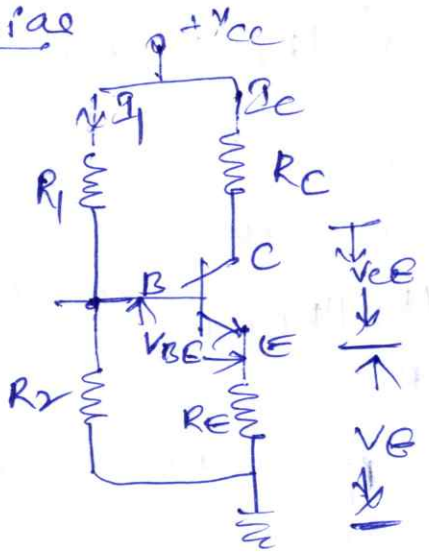



→ stability factor, S for fixed bias ckt

$$S = 1+\beta.$$

→ stability factor of this circuit is high, there by indicating unstability

Self Bias

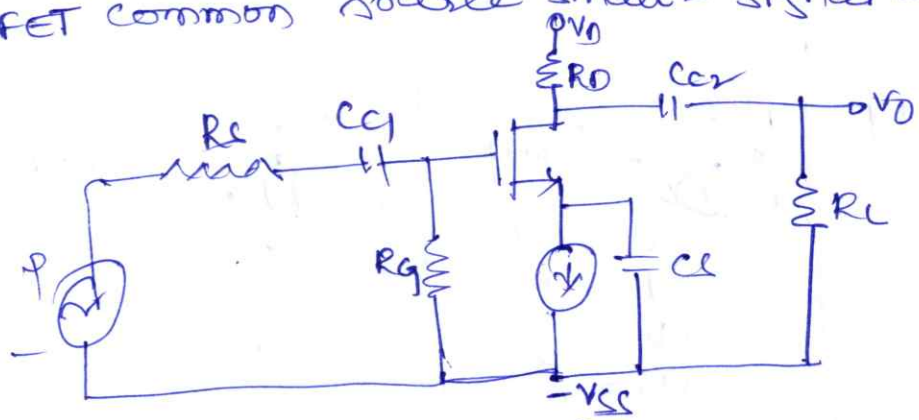



⇒ stability factor, S for self bias is

$$S = \frac{(1+\beta)\left(1+\frac{R_{Th}}{R_E}\right)}{1+\beta\left(\frac{R_{Th}}{R_E}\right)}$$

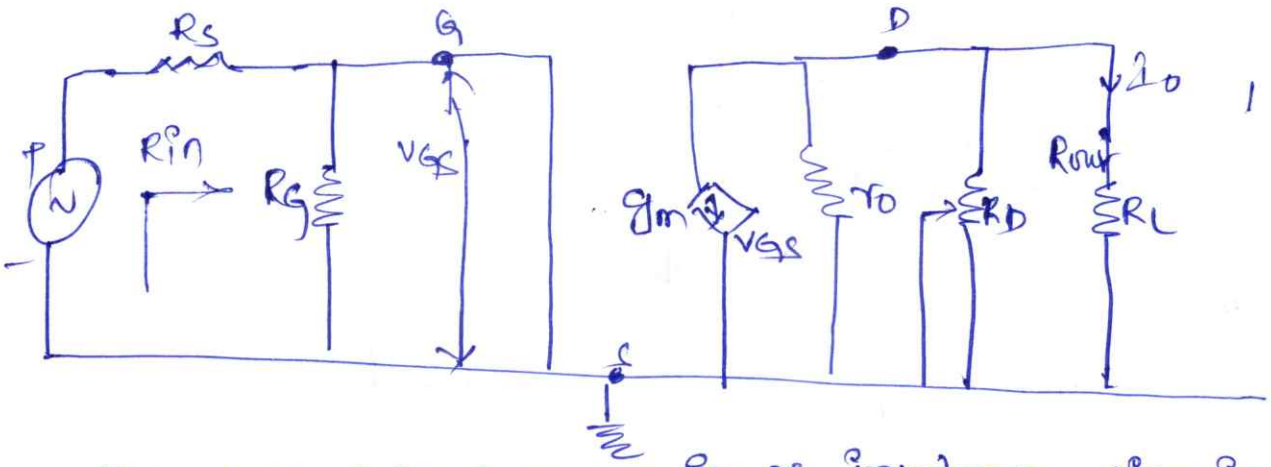
⇒ stability factor of this ckt is much small when compared to the other fixed

(6) MOSFET common source small-signal Amplifier




→ Here, $C_{C_1}$ & $C_{C_2}$ are coupling capacitors & the $C_S$ is bypass capacitor

Analysis of Small Signal equivalent circuit for the common Source MOSFET Amp




Here we calculate the i/p, o/p impdance. circuit & voltage gain similar to BJT & FET

→ i/p impdence $R_{in} = R_G$

→ o/p " $R_{out} = r_o \| R_D$ (when $V_s = 0 \Rightarrow g_m V_{gs} = 0$)

→ Voltage gain $A_v = \frac{v_o}{v_i} \Rightarrow A_v = -g_m (r_o \| R_D \| R_L)$

→ overall volt gain; $G_v = \frac{v_o}{v_s} = \frac{v_o}{v_i} \cdot \frac{v_i}{v_s} = A_f \frac{v_i}{v_s}$

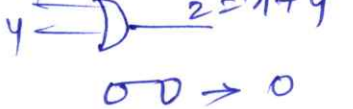
$$G_v = \frac{-g_m (r_o \| R_D \| R_L) \cdot R_G}{R_G + R_s}$$

→ current gain, $A_i = \frac{i_o}{i_i} \Rightarrow$ At the i/p $V_{GS} = i_i R_G$

$$A_{i_o} = \frac{i_o}{i_i} = \frac{-r_o \| R_D}{r_o \| R_D + R_L} g_m R_G.$$

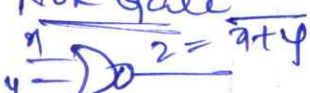
=

7 a) OR Gate



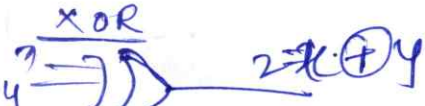

00 → 0
01 → 1
10 → 1
11 → 1

NOR Gate




00 → 1
01 → 0
10 → 0
11 → 0

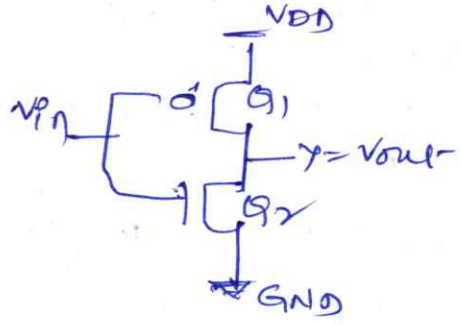
XOR




00 → 0
01 → 1
10 → 1
11 → 0

=

7 B CMOS (complementary metal oxide - s/c), it consists of PMOS & NMOS Transistor.




| Vin | Q1 | Q2 | Vout |
|---|---|---|---|
| 0.0 (L) | OFF | ON | 5.0 (H) |
| 5.0 (H) | OFF | ON | 0.0 (L) |

Case(i) When i/p is low $\Rightarrow V_{out} = V_{DD}$

Case(ii) When i/p is high $\Rightarrow V_{out} = 0\ V$

8

$F(A,B,C,D) = A'BD' + ACD + B'CD + AB'C'D$, SOP & POS

find 'F' → Evaluate F for all 16 combination (A,B,C,D) the F is 1 for the following minterms.

0000 → $m_0$
0001 → $m_1$
0011 → $m_3$
0100 → $m_4$
0101 → $m_5$
0110 → $m_6$
1011 → $m_{11}$
1111 → $m_{15}$

$F = \sum m(1,3,4,5,6,11,15)$

→ canonical SOP

$f = m_1 + m_3 + m_5 + m_6 + m_{11} + m_{15}$

$F = A'B'C'D + AB'CD + A'BC'D + A'BCD' + ABC'D + ABCD$

⇒ canonical POS = function

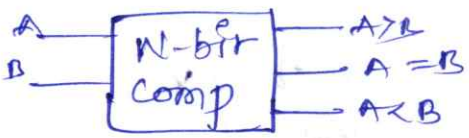
$\{0, 2, 7, 8, 9, 10, 12, 13, 14\}$

$F = \prod M(0, 2, 7, 8, 9, 10, 12, 13, 14)$

$F = (A+B+C+D)(A+B+C'+D)(A+B'+C'+D)$
$(A'+B+C+D)(A'+B+C'+D)(A'+B+C+D')(A'+B'+C+D)$
$(A'+B'+C'+D)(A'+B'+C'+D')$

$M_0, M_2, M_7, M_8, M_9, M_{10}, M_{12}, M_{13}, M_{14}$

(9) 2-bit comparator using gates




Here $A = A_1 A_0$, $B = B_1 B_0$

E=1 when A=B

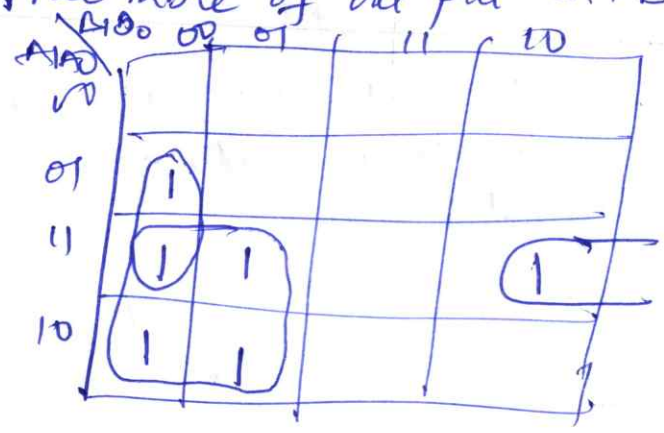
G=1 when A>B

L=1 when A<B.

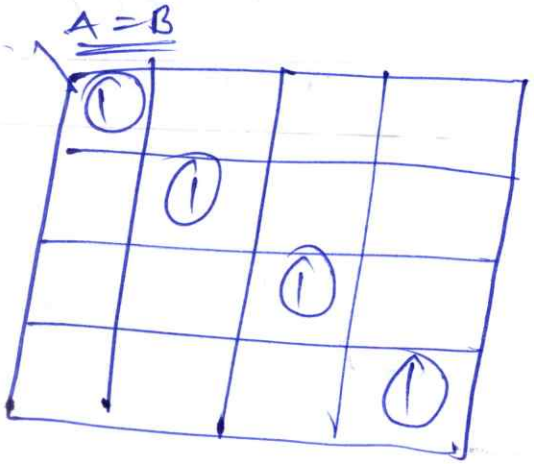
2-bit comparator used to compare 2 binary no. of each bits called a 2bit magnitude comperator.

| Inputs | | | | outputs | | |
|---|---|---|---|---|---|---|
| $A_1$ | $A_0$ | $B_1$ | $B_0$ | A<B | A=B | A>B |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |

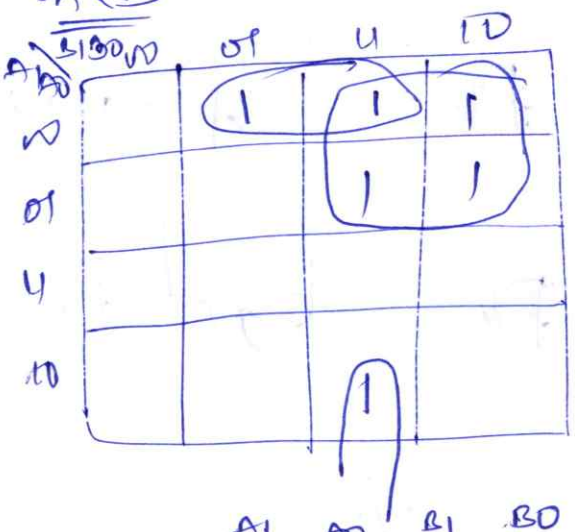
True Table of output - A>B.




A=B



A<B

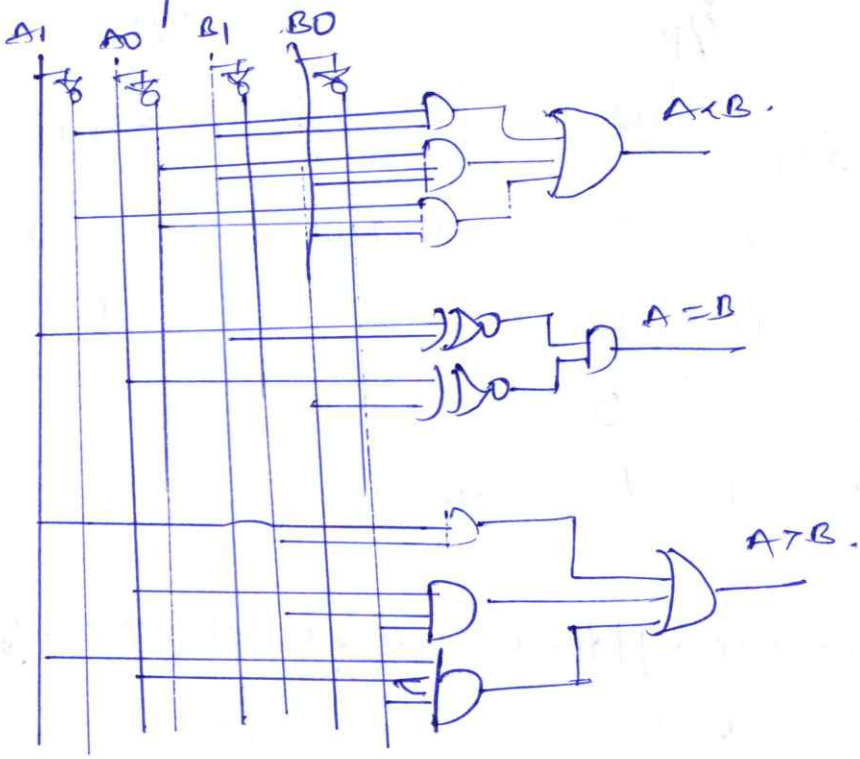



$A>B = A_1B_1' + A_0B_1'B_0' + A_1A_0B_0'$

$A=B = A_1'A_0'B_1'B_0' + A_1A_0B_1'B_0 + A_1A_0B_1B_0 + A_1A_0'B_1B_0'$

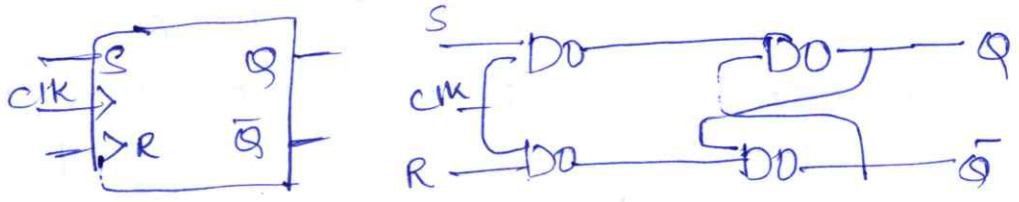
$= A_0 (Ex\text{-}NOR\ B_0)(A_1\ Ex\text{-}NOR\ B_1)$

$A<B = A_1'B_1 + A_0'B_1B_0 + A_1'A_0'B_0$




(10)

S-R flip-flop :- circuit representation of clocked S-R FF using NAND.

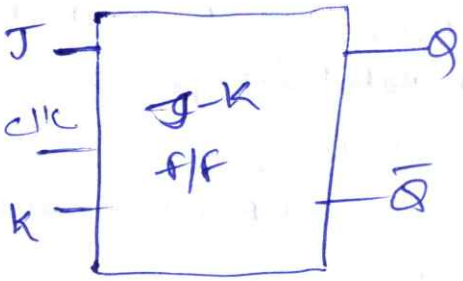


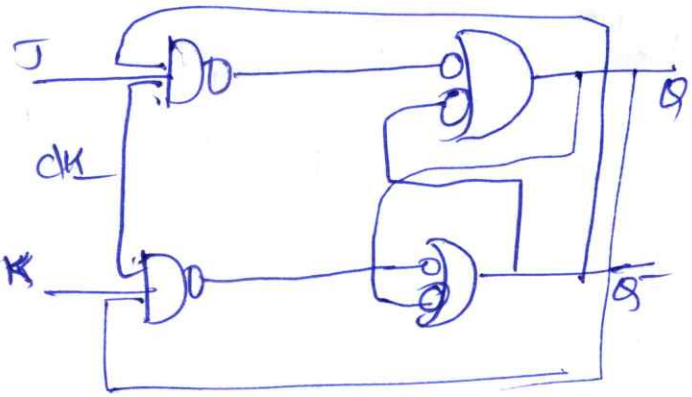

Case (i)

Case i) S=0 R=0 → Hold mode.
(ii) S=0 R=1 → Reset mode
(iii) S=1 R=0 → set mode
(iv) S=1 R=1 → invalid state

| S | R | $Q_{n+1}$ |
|---|---|---|
| 0 | 0 | $Q_n$ |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | indeterminate |

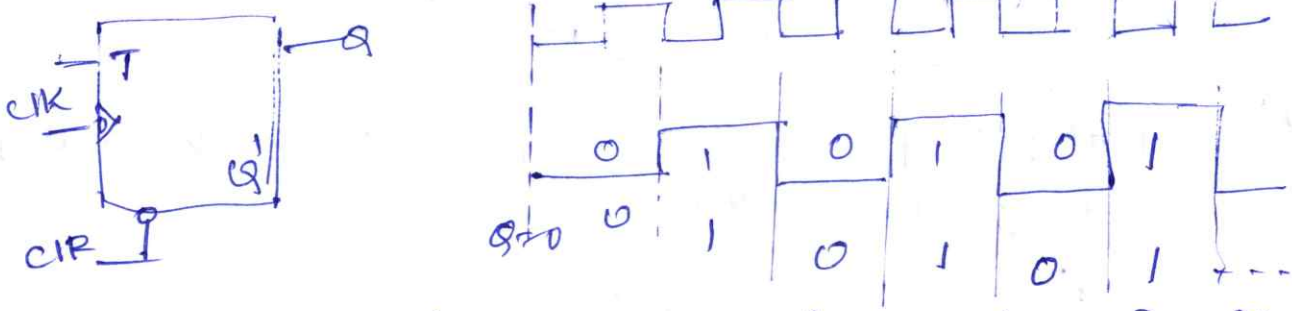
## J-K flip flop's




| operating mode | i/p CLK. | J | K | o/p Q | Effect on o/p Q. |
|---|---|---|---|---|---|
| Hold | ⊓ | 0 | 0 | No change | No change / disable |
| Reset | ⊓ | 0 | 1 | 0 | Reset to 0 |
| Set | ⊓ | 1 | 0 | 1 | Set to 0 |
| Toggle | ⊓ | 1 | 1 | Toggle | change opposite state |

(4) Asynchronous up/down counter using JK f/f.




when -ve edge clock pulse is applied & i/p is OFF
logic = 1
the o/p f/f will Toggle for every falling edge

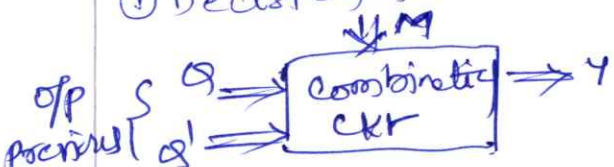
(*) Design of 3-bit Asynchronous up/down counter.

① It has a mode control i/p (say M) is used for selecting up & down mode.

② A combinational circuit is required b/w each pair of f/f to decide whether to do up or down counting.

for $n=3 \Rightarrow$ max count $= 2^3 - 1$

① Decision for mode control i/p




When m=0 then $Y = Q \Rightarrow$ up counter

When m=1 then $Y = Q' \Rightarrow$ down counter

| m | Q | Q' | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

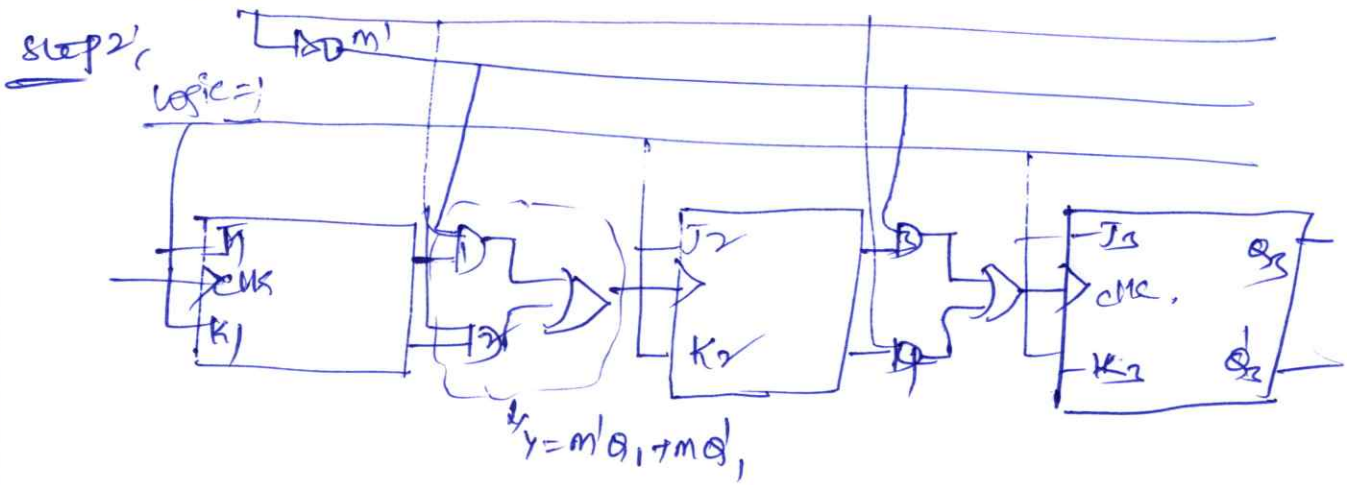
m

| m \ QQ' | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 |

$Y = A + B$

$Y = m'Q + mQ'$

Step 2:




Timing diagram (initially $Q_3=0$ $Q_2=0$ $Q_1=0$)