Code No.: R22EC301ES	R22	H.T.No.			8	R					

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Regular) - December- 2025
ANALOG & DIGITAL ELECTRONICS
(Common for IT, CSM)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a)	Draw V-I characteristic of a p-n junction diode.	[1M]
b)	Why is rectifier so named?	[1M]
c)	What is an amplifier?	[1M]
d)	Why biasing is necessary in amplifier circuits?	[1M]
e)	Define the threshold voltage of a n-channel enhancement MOSFET.	[1M]
f)	Draw basic CMOS logic circuit.	[1M]
g)	What are the universal gates? Why they are called universal gates?	[1M]
h)	List out the applications of multiplexer.	[1M]
i)	Compare shift registers and ripple counters.	[1M]
j)	What are programmable memories?	[1M]

PART-B **(50 Marks)**

2.a)	Derive diode current equation.	[5M]
b)	A silicon diode has a saturation current of 7.5μA at room temperature 300 K. Calculate the saturation current at 400K.	[5M]
	OR	
3.	Explain the operation of Full wave rectifier and derive the expression for ripple factor of a full-wave center-tap rectifier with capacitor filter.	[10M]
4.	Derive the equation for the overall voltage gain of a multistage CE amplifier.	[10M]
	OR	
5.a)	What is DC load line and AC load line? Explain the criteria for fixing operating point.	[5M]
b)	Explain the fixed bias and self-bias circuits in detail.	[5M]
6.	Illustrate in detail about small- signal model of MOSFET.	[10M]
	OR	
7.a)	With the help of truth tables and discuss the functionality of the following logic gates: (i) OR Gate. (ii) NOR Gate. and (iii) XOR Gate.	[5M]
b)	Draw the circuit diagram of basic CMOS Gate and explain its operation.	[5M]
8.	Obtain the Standard POS and SOP expressions for the function F(A,B,C,D) = A'BD'+ACD+B'CD+A'C'D.	[10M]
	OR	
9.	Design a 2-bit comparator using gates.	[10M]
10.	Draw the logic symbol, characteristics table and derive characteristics equation of S-R and J-K flip-flop.	[10M]
	OR	
11.	Design Asynchronous up/down counter using JK flip-flop.	[10M]

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