Code No.: EC744PE	R20	H.T.No.			8	R						

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
IV–B.TECH–I–Semester End Examinations (Supply) - December- 2025
DIGITAL CMOS IC DESIGN
(ECE)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Define Threshold Voltage.	[2M]
b)	Define CMOS inverter logic.	[2M]
c)	Differentiate between NMOS and CMOS.	[2M]
d)	Short note on complex logic circuits.	[2M]
e)	Draw the circuit diagram of D latch.	[2M]
f)	Write short note latch and flip flop.	[2M]
g)	Any two Advantages of CMOS gates.	[2M]
h)	Define dynamic CMOS logic circuits.	[2M]
i)	What are the types of semiconductor memories?	[2M]
j)	What is meant by DRAM cells?	[2M]

PART-B **(50 Marks)**

2.	Determine the pull-up to pull-down ratio for an NMOS inverter.	[10M]
	OR	
3.	Write a short note on Transistor equivalency.	[10M]
4.	Discuss the transient analysis of the CMOS transmission gate by replacing it with a resistor equivalent circuit.	[10M]
	OR	
5.	How the MOS inverters connected in cascade can drive large capacitive loads? Explain.	[10M]
6.	Draw the edge triggered D flip-flop by using CMOS logic and explain its operation in detail.	[10M]
	OR	
7.	Explain behavior of bistable elements.	[10M]
8.	Explain voltage bootstrapping with an example.	[10M]
	OR	
9.	Write a short note on High performance Dynamic CMOS circuits.	[10M]
10.	Explain the principle of NAND gate flash memory with a neat diagram.	[10M]
	OR	
11.	Discuss about sources of leakage current in SRAM.	[10M]

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