Code No.: DS305ES	R20	H.T.No.			8	R					

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Supply) - December- 2025
DIGITAL LOGIC DESIGN
(CSD)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1.	a)	Convert the $(7BD)_{16}$ hexadecimal number to decimal.	[2M]
	b)	Prove that x+x'y=x+y.	[2M]
	c)	Reduce the Boolean expression f (x, y, z)=∑m(1, 3, 5,7).	[2M]
	d)	Draw the logic diagram of EXOR using NOR gate.	[2M]
	e)	Compare combinational and sequential circuits.	[2M]
	f)	Design 4X1 MUX.	[2M]
	g)	How to avoid race around condition?	[2M]
	h)	Compare synchronous and asynchronous counters.	[2M]
	i)	Explain the random-access memory.	[2M]
	j)	Explain the programable array logic.	[2M]

PART-B **(50 Marks)**

2.	Convert the $(776)_8$ octal number to decimal and also binary number. Subtract $(7B)_{16}$ from $(C4)_{16}$ using 2s complements method.	[10M]
	OR	
3.	Convert the following Boolean expression into canonical SOP and POS for F(X, Y, Z)=Y'+ZX'+X'Y+Z.	[10M]
4.	Simplify the following Boolean expression using K Map. F(A,B,C,D)=∑m(0,1,4,5,8,9,13,15. F(A,B,C,D)=∑m(1,3,4,9,13)+ω(2,6,12).	[10M]
	OR	
5.	Reduce the Boolean expression using K-map and implement expression in NAND gates F(A,B,C,D)=∑m(1,3,5,9,11)+ω(2,4,8).	[10M]
6.	Design a full adder.	[10M]
	OR	
7.	Design Half adder using NAND Gates.	[10M]
8.	Explain the T flip flop with characteristic table and excitation table.	[10M]
	OR	
9.	Design synchronous 3bit counter using J K Flip Flop.	[10M]
10.	Explain the Programmable Logic Array.	[10M]
	OR	
11.	Explain the memory decoding.	[10M]

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