

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS

II-B.TECH-I-Semester End Examinations (Regular) - December- 2025
DIGITAL LOGIC DESIGN
(ECE)

[Time: 3 Hours]

[Max. Marks: 60]

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 10 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A

(10 Marks)

1. a)	State the duality theorem.	[1M]
b)	Given that $(432.354)_{10} = (X)_2$, Determine the value of X.	[1M]
c)	Write the TTL characteristics.	[1M]
d)	Draw the NOT gate using CMOS logic.	[1M]
e)	Define preset and clear inputs.	[1M]
f)	Write any two differences between combinational and sequential circuits.	[1M]
g)	How many states are there in a n-bit ring counter?	[1M]
h)	Define right shift register.	[1M]
i)	What is FSM?	[1M]
j)	Define merger graph.	[1M]

PART-B

(50 Marks)

2.	Explain about binary number systems and BCD codes with example.	[10M]
OR		
3.a)	Determine the standard sum-of-products representation of the following functions.	[5M]
$f(x, y, z) = z + (\bar{x} + y)(x + \bar{y})$		
b)	Realize the AND, OR and NOT gates using NAND gate.	[5M]
4.	Minimize the following function using K-Map and draw the logic diagram.	[10M]

$$f(v, w, x, y, z) = \sum m(1, 2, 6, 7, 9, 13, 14, 15, 17, 22, 23, 25, 29, 30, 31)$$

OR

5.	Realize a NAND and NOR gates using CMOS logic.	[10M]
6.	Design a BCD-to-decimal decoder.	[10M]
7.	Realize the given function using 8x1 MUX.	[10M]

$$F(A, B, C, D) = \sum (1, 2, 5, 6, 7, 8, 10, 14, 15)$$

8.	Design a 4-bit Ring counter and explain its operation.	[10M]
OR		
9.	Implement the state diagram and state stable for a parity-bit generator.	[10M]

10. Find the stat equivalence and the corresponding reduced machine [10M]

<i>PS</i>	<i>NS, z</i>	
	<i>x = 0</i>	<i>x = 1</i>
<i>A</i>	<i>B, 0</i>	<i>E, 0</i>
<i>B</i>	<i>E, 0</i>	<i>D, 0</i>
<i>C</i>	<i>D, 1</i>	<i>A, 0</i>
<i>D</i>	<i>C, 1</i>	<i>E, 0</i>
<i>E</i>	<i>B, 0</i>	<i>D, 0</i>

OR

11. Analyze the procedure of state minimization using the merger graph with example. [10M]
