Code No.: EC301PC	R20	H.T.No.			8	R						

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Supply) - December- 2025
ELECTRONIC DEVICES AND CIRCUITS
(ECE)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	What is peak inverse voltage?	[2M]
b)	Distinguish between avalanche and Zener mechanisms of a diode.	[2M]
c)	What is thermal runway?	[2M]
d)	What is the need of biasing?	[2M]
e)	List out the applications of FET.	[2M]
f)	What is pinch-off voltage?	[2M]
g)	Why a capacitive coupling used to connect signal source to an amplifier?	[2M]
h)	Draw Small signal low frequency transistor Models.	[2M]
i)	What are the different types of FETs?	[2M]
j)	Draw JFET transistor small signal low frequency hybrid model.	[2M]

PART-B **(50 Marks)**

2.a)	Draw and explain the graph indicating the variation of minority carrier density with distance in a p-n junction diode under forward biased condition.	[5M]
b)	Explain how Zener diode act as a voltage regulator	[5M]
	OR	
3.a)	Draw and explain the circuit of a half-wave rectifier with capacitor filter.	[5M]
b)	Explain the design of Full wave with bridge rectifier.	[5M]
4.	Draw the Self bias circuit and derive the stability factor for it along with explanation.	[10M]
	OR	
5.	Explain various current components in Bipolar Junction Transistor.	[10M]
6.a)	Write the construction, operation and characteristic behavior of JFET.	[5M]
b)	Compare the BJT and FET transistors.	[5M]
	OR	
7.	Discuss the operation and characteristics of the following: i) Tunnel diode. ii) Photo diode.	[10M]
8.	Draw and explain the h-parameter equivalent circuit of a transistor in CE configuration. Derive the expressions for input impedance, output impedance, voltage gain and current gain.	
	OR	
9.	The hybrid parameters for a transistor used in CE configuration are h_{ie} = 5kΩ; h_{fe} = 180; h_{re} = 1.25 × 10-4; h_{oe} = 16 × 10-6 ohms. The transistor has a load resistance of 20 KΩ in the collector and is supplied from a signal source of resistance 5 KΩ. Compute the value of input impedance, output impedance, current gain and voltage gain.	[10M]

10.a) Give the advantages of h-parameter analysis. [5M]

b) Write short notes on Small Signal Model of JFET. [5M]

OR

11. Define and explain the parameters trans-conductance (g_m) drain resistance (r_d) and amplification factor (μ) of a JFET and establish a relation between them. [10M]

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