

CMR ENGINEERING COLLEGE: : HYDERABAD

UGC AUTONOMOUS

III–B.TECH–II–Semester End Examinations (Supply) - December- 2025

FPGA PROGRAMMING

(ECE)

[Time: 3 Hours]

[Max. Marks: 70]

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 20 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A**(20 Marks)**

1. a) Specify the main advantage of a Masked Gate Array ASIC over other SPLDs? [2M]
- b) What is the purpose of Clock Drivers in CPLDs? [2M]
- c) Summarize the purpose of a Specification Review? [2M]
- d) What is the basic structure of a VHDL module? [2M]
- e) Organize different styles of hardware description in HDLs? [2M]
- f) What is the role of the IF statement in Behavioral Descriptions? [2M]
- g) Interpret the Structural Description in the context of HDLs? [2M]
- h) What are some examples of serial and parallel combinations of switches in switch level description? [2M]
- i) Differentiate between Procedures and Tasks in HDLs. [2M]
- j) Define the word “simulation”, and how is it used in verification? [2M]

PART-B**(50 Marks)**

2. Describe the structure and functionality of Programmable Logic Arrays (PLAs). How do they differ from Programmable Array Logic (PAL) devices? [10M]

OR

3. Detail the architecture of FPGAs, focusing on Configurable Logic Blocks (CLBs), Configurable I/O Blocks. [10M]

4. Explain the Universal Design Methodology (UDM) and its importance in the design of programmable devices. [10M]

OR

5. Discuss the role of Hardware Descriptive Languages (HDLs) in Top-Down Design. [10M]

6. Create a VHDL Dataflow Description for a 4-bit magnitude comparator. Include constant declarations and assignments. [10M]

OR

7. Explain the structure of a Behavioral description Model in VHDL. [10M]

8. Build a VHDL program to describe a 4-bit ripple carry adder using Structural Description. [10M]

OR

9. Explain the significance of Switch-Level Description in HDLs. How does Switch-Level Description contribute to the modeling of complex digital circuits? [10M]

10. Write a Verilog task to perform binary to gray code conversion. Explain the inputs and outputs of this task. [10M]

OR

11. Discuss the role of static timing analysis in HDL design. What tools are commonly used? [10M]
