

**CMR ENGINEERING COLLEGE: : HYDERABAD**  
**UGC AUTONOMOUS**

**III-B.TECH-II-Semester End Examinations (Supply) - December- 2025**  
**VLSI DESIGN**  
**(ECE)**

**[Time: 3 Hours]**

**[Max. Marks: 70]**

**Note:** This question paper contains two parts A and B.

Part A is compulsory which carries 20 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b, c as sub questions.

**PART-A**

**(20 Marks)**

1. a)	Draw the characteristics of CMOS inverter.	[2M]
b)	Define $g_m$ of MOS transistor.	[2M]
c)	What is stick diagram?	[2M]
d)	Define layout.	[2M]
e)	What is mean by fan-in and fan-out?	[2M]
f)	List the sources of wiring capacitance.	[2M]
g)	Explain the difference between EPROM and EEPROM.	[2M]
h)	Draw the circuit diagram of one transistor DRAM.	[2M]
i)	What are programmable logic devices?	[2M]
j)	Why the chip testing is needed?	[2M]

**PART-B**

**(50 Marks)**

2.a)	Derive the relationship between $I_{ds}$ and $V_{ds}$ .	[7M]
b)	Compare Bipolar and CMOS Technologies.	[3M]

**OR**

3.	Derive pull-up to pull-down ratio for nMOS inverter driven by another nMOS inverter.	[10M]
4.a)	Define Scaling? Explain the different Scaling parameters of MOS circuits along with Limitations of Scaling.	[7M]
b)	Why the design rules should be followed for layout design.	[3M]

**OR**

5.	Draw and explain the CMOS lambda based design rules for transistors.	[10M]
6.	What are the alternate gate circuits available? Explain any one of them with suitable sketch by taking NAND gate as an example.	[10M]

**OR**

7.a)	What is dynamic logic? Explain its basic gate functionality.	[5M]
b)	What are the different complex logic gates and compare their performance in all aspects.	[5M]

8.a)	Draw the basic circuit diagram of static RAM cell.	[5M]
b)	Draw the basic block diagram of 4-bit adder and explain its operation in detail.	[5M]

**OR**

9.a)	Draw the circuit diagram for 4-bit ALU and explain its operation in detail.	[6M]
b)	Compare SRAM and DRAM.	[4M]

10.	Explain the Design Strategies for test in a CMOS circuits and explain its operation.	[10M]
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**OR**

11.a)	Differentiate PAL and PLA.	[6M]
b)	Explain about standard cells.	[4M]