Code No.: R22EC603PC

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CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
III–B.TECH–II–Semester End Examinations (Supply) - December- 2025
VLSI DESIGN
(ECE)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a)	Define MOS transistor figure of merit.	[1M]
b)	List the advantages of BiCMOS.	[1M]
c)	Define stick diagram.	[1M]
d)	What is meant by scaling factor?	[1M]
e)	Mention the advantages of transmission gate.	[1M]
f)	Define fan in of CMOS logic gate.	[1M]
g)	Write the sum expression for 2-bit adder.	[1M]
h)	Draw a DRAM memory cell.	[1M]
i)	Define programmable logic array.	[1M]
j)	What is meant by struck at 1 fault?	[1M]

PART-B **(50 Marks)**

2.	Derive the drain to source current (I_{ds}) and drain to source voltage(V_{ds}) expression for n-MOS transistor.	[10M]
	OR	
3.	Describe the operation and transfer characteristics of n-MOS inverter.	[10M]
4.	Derive supply voltage, channel width, channel length, gate oxide thickness, and gate area and gate capacitance using constant electric field scaling.	[10M]
	OR	
5.	Draw a layout diagram CMOS inverter and 2 inputs CMOS NAND gate with lambda values.	[10M]
6.	Discuss inverting and non-inverting type n-MOS super buffer with neat sketches.	[10M]
	OR	
7.a)	Implement Y= AB+C using pass transistors.	[5M]
b)	Implement Y=A+B using Transmission gate.	[5M]
8.	Design a serial multiplier with neat diagrams.	[10M]
	OR	
9.	Explain the operation of 6T SRAM memory cell.	[10M]
10.	Discuss in detail about chip level design techniques.	[10M]
	OR	
11.	Explain in detail about FPGA architectures.	[10M]

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