I-M.TECH-I-Semester End Examinations (Regular) - February-2026

CMOS ANALOG IC DESIGN (VLSI SD)

PART-A (10 Marks)

1(a) Body Effect in MOSFET

When the source-to-body voltage (Vsb) is non-zero, the depletion region widens and the threshold voltage increases.

The modified threshold voltage is given by:

$V_T = V_{T0} + \gamma(\sqrt{(2\varphi_F + V_{sb})} - \sqrt{(2\varphi_F)})$.

As Vsb increases, VT increases, reducing overdrive voltage and drain current.

This effect is significant in analog design where source is not at ground potential.

1(b) Output Swing in Resistive CS Amplifier

The maximum output voltage is approximately VDD.

The minimum output voltage is limited by saturation condition $V_{DS} \geq V_{ov}$.

Hence $V_{out(min)} \approx V_{ov}$.

Therefore output swing is limited by supply rails and saturation requirement of the MOS transistor.

1(c) CMRR

CMRR is defined as Ad/Acm and in dB equals 20log(Ad/Acm).

It measures the ability of a differential amplifier to reject common-mode signals.

It is mainly limited by finite tail current source resistance and device mismatch.

1(d) Compliance Voltage of Cascode Mirror

Minimum output voltage required to keep both devices in saturation equals sum of overdrive voltages.

$V_{out(min)} \approx V_{ov1} + V_{ov2}$.

This limits output swing but improves output resistance significantly.

1(e) Gain Boosting

Gain boosting increases effective output resistance by amplifying the cascode gate node variations.

Effective output resistance becomes $A_{boost} \cdot r_o$, increasing DC gain without stacking more devices.

Formula: $r_{out,eff} = A_{boost} \cdot r_o$

PART-B (50 Marks)

2(a): Velocity Saturation in Short-Channel MOSFETs

In long-channel MOSFETs, the drain current in saturation region is derived using the gradual channel approximation. The drain current equation is:

$I_D = (1/2)\ \mu C_{ox}\ (W/L)(V_{GS} - V_T)^2$.

This quadratic relationship assumes that carrier drift velocity increases linearly with electric field, i.e., $v=\mu E$

where μ is carrier mobility.

*Onset of Velocity Saturation:

As channel length L decreases in deep submicron technologies, the lateral electric field near the drain becomes very high. When the electric field

exceeds a critical value E_c, carriers reach a maximum velocity called saturation velocity v_{sat}. Beyond this point: $v \approx v_{sat}$

Thus, carrier velocity no longer increases linearly with electric field.

*Modified Drain Current Expression:

Under velocity saturation, drain current becomes:

$I_D \approx WC_{ox} (V_{GS}-V_T)v_{sat}$

Here, current varies linearly with overdrive voltage Vov, unlike the quadratic dependence in long-channel devices.

*Impact on Analog Performance:

1)Reduced Transconductance g_m:

In long-channel devices, $g_m=(2.I_D)/Vov$

But under velocity saturation,

$g_m \approx WCox.v_{sat}$

Thus, g_m becomes independent of Vov.

2)Lower Intrinsic Gain:

Since intrinsic gain = $g_m r_o$, reduction in g_m decreases amplifier gain.

3)Reduced Output Resistance:

Short-channel effects increase channel length modulation.

4)Degraded Linearity:

Linear current relation affects distortion behavior.

2(b): Drain Current Calculation Including Channel Length Modulation

Given:

$V_{GS}=3.5V$

$V_T=1V$

$V_{DS}=5V$

$K_n=250\mu A/V^2$

$\lambda=0.02V^{-1}$

Step 1: Determine Region of Operation

First calculate overdrive voltage:

$V_{OV}=V_{GS}-V_T$

$V_{OV}=3.5-1=2.5V$

For saturation region: $V_{DS} \geq V_{OV}$

Since: $5V>2.5V$

The MOSFET operates in saturation region.

Step 2: Drain Current Expression

Including channel length modulation, the drain current in saturation is:

$I_D=1/2\ K_n\ (V_{OV})^2\ (1+\lambda V_{DS})$

Substituting values:

$I_D=1/2(250)(2.5)^2\ (1+0.02\times5)$

$I_D=125\times6.25\times(1+0.1)$

$I_D=125\times6.25\times1.1$

$I_D=859\mu A(approx.)$

Step 3: Interpretation

The term $(1+\lambda V_{DS})$ accounts for channel length modulation, which slightly increases the drain current due to effective channel shortening. Without this effect, current would be slightly lower. This demonstrates

how short-channel effects influence practical MOSFET behavior in analog circuits.

OR

3(a): Trade-Offs in MOS Device Models :

In analog CMOS design, accurate modeling of MOSFET behavior is essential for predicting circuit performance. Different device models are used depending on the required accuracy and complexity. The primary trade-off exists between simplicity and precision.

1) Square-Law (Long-Channel) Model

For a MOSFET operating in saturation:

$I_D=1/2\ \mu C_{ox}\ W/L(V_{GS}-V_T)^2$

This model is derived using the gradual channel approximation and assumes constant mobility and no short-channel effects.

*Advantages:

1.Simple mathematical form.

2.Easy for hand derivations.

3.Suitable for exam calculations.

4.Helps in understanding basic device physics.

*Limitations:

1.Ignores velocity saturation.

2.Does not consider channel length modulation properly.

3.No DIBL (Drain Induced Barrier Lowering).

4.Inaccurate for modern deep submicron CMOS.

2) Advanced Models (BSIM Model):

Modern technologies use BSIM (Berkeley Short-channel IGFET Model), which includes:

->Channel length modulation

->Velocity saturation

->Mobility degradation

->Body effect

->DIBL

->Subthreshold conduction

*Advantages:

1.Highly accurate.

2.Suitable for nanometer CMOS.

3.Required for circuit simulation and tape-out.

*Limitations:

1.Very complex equations.

2.Not suitable for manual calculations.

3.Requires simulation tools.

For theoretical derivations and conceptual clarity, the square-law model is sufficient. However, for practical IC design and accurate prediction of circuit behavior, advanced models like BSIM are mandatory. Thus, designers must balance analytical simplicity with physical accuracy depending on the application.

3(b): Importance of Second-Order Effects in MOSFETs :

In modern CMOS technologies, especially deep submicron processes, second-order effects significantly influence MOSFET behavior. While the ideal square-law model assumes constant mobility and infinite output resistance, practical devices exhibit deviations due to scaling. These second-order effects are crucial in analog circuit design because they directly affect gain, linearity, and stability.

1. Channel Length Modulation (CLM)

In saturation, the effective channel length shortens as V_{DS} increases. Hence drain current slightly increases even in saturation:

$I_D=1/2\ \mu C_{ox}\ W/L(V_{OV})^2\ (1+\lambda V_{DS})$

This introduces finite output resistance:

$r_o=1/(\lambda I_D)$

Reduced r_o lowers intrinsic gain ($g_m r_o$), limiting amplifier gain.

2. Velocity Saturation

At high electric fields, carrier velocity saturates at v_{sat}, making drain current linear in V_{OV}. This reduces transconductance g_m compared to long-channel prediction, decreasing gain.

3. Drain Induced Barrier Lowering (DIBL)

High drain voltage lowers threshold voltage, increasing leakage and reducing device control. This impacts bias stability and increases distortion.

4. Mobility Degradation

At high vertical electric fields, mobility decreases due to surface scattering, reducing current drive capability.

Second-order effects reduce intrinsic gain, affect linearity, increase leakage, and degrade analog performance. Therefore, they must be considered carefully in modern CMOS analog circuit design, especially in scaled technologies where these effects dominate device behavior.

4(a): Frequency Response of Common-Gate Amplifier:

The common-gate (CG) amplifier is widely used in high-frequency analog applications due to its wide bandwidth and absence of Miller effect. In this configuration, the gate terminal is AC grounded, the input is applied to the source, and the output is taken from the drain.

1. Small-Signal Voltage Gain

For a CG amplifier operating in saturation: $A_v=g_m R_D$

where g_m= transconductance, R_D= drain resistance

Unlike the common-source amplifier, there is no phase inversion.

2. Input Resistance

The input resistance is given by:

$R_{in}=1/g_m$

Since g_m is typically large, R_{in} is small. This makes the CG amplifier suitable for low-impedance sources such as RF inputs.

3. Frequency Response

Because the gate is AC grounded, the gate-to-drain capacitance C_{gd} does not undergo Miller multiplication. Hence, the effective input capacitance is

small. The dominant pole is mainly determined by the output node:

$f_p=1/(2\pi R_{out}.C_L)$

where C_L is load capacitance.

Due to absence of Miller effect, the bandwidth of CG amplifier is significantly higher than common-source configuration.

4. Advantages and Applications

->High bandwidth

->Good input-output isolation

->Suitable for RF front-end amplifiers

->Wideband amplification

The common-gate amplifier provides moderate gain but very high bandwidth. Its low input impedance and reduced Miller capacitance make it highly suitable for high-frequency and RF analog circuit applications.

4(b): Gain-Bandwidth-Power Trade-Off in Analog Amplifiers :

In analog CMOS design, gain, bandwidth, and power consumption are interdependent parameters. Improving one often degrades the others. Understanding this trade-off is essential in amplifier design.

1. Voltage Gain

For a MOS amplifier: $A_v=g_m r_o$

where g_m= transconductance, r_o= output resistance

Higher gain requires either large g_m or large r_o.

2. Bandwidth

The dominant pole frequency is:

$f_p = 1/(2\pi R_{out} C_L)$

Gain-bandwidth product (GBW) is approximately:

$GBW = g_m/(2\pi C_L)$

Thus, bandwidth increases with transconductance.

3. Power Consumption

Transconductance is related to bias current:

$g_m = (2I_D)/V_{OV}$

To increase g_m, drain current $I_D$must increase, which raises power consumption: $P = V_{DD} \cdot I_D$

4. Trade-Off Explanation

->Increasing gain by increasing r_o(using longer channel devices) reduces bandwidth.

->Increasing $g_m$improves bandwidth but increases power.

->Cascoding improves gain but reduces output swing and bandwidth.

->Larger devices increase capacitance, reducing speed.

Designers must balance gain, bandwidth, and power depending on application requirements. High-speed circuits prioritize bandwidth and accept higher power, while low-power designs sacrifice gain and bandwidth. Efficient analog design involves optimizing these competing parameters.

OR

5(a): Common-Gate Amplifier as a Low Input Impedance Stage :

The common-gate (CG) amplifier is widely used in analog and RF design when a low input impedance stage is required. In this configuration, the gate terminal is AC grounded, the input signal is applied at the source, and the output is taken from the drain.

1. Input Resistance Derivation:

From small-signal analysis, the input resistance of a common-gate amplifier is: $R_{in}=1/g_m$

where g_m is the transconductance of the MOSFET.

Since transconductance is given by: $g_m=(2I_D)/V_{OV}$

a reasonably biased MOSFET has a large g_m, which results in very small input resistance. Thus: $R_{in}\rightarrow$"small"

This makes CG amplifier ideal for low-impedance signal sources.

2. Voltage Gain:

The voltage gain of a CG amplifier is: $A_v=g_m R_D$

Unlike the common-source amplifier, there is no phase inversion.

3. Advantages of Low Input Impedance:

->Provides impedance matching for RF circuits (e.g., 50Ω systems).

->Reduces reflection in high-frequency transmission lines.

->Minimizes loading effects in current-mode circuits.

->Suitable for wideband applications due to absence of Miller effect.

4. Applications:

->RF front-end amplifiers

->Low-noise amplifiers (LNA)

->Current buffers

->Wideband amplifiers

The common-gate amplifier is preferred when low input impedance and high bandwidth are required. Its simple input resistance expression $R_{in}=1/g_m$ makes it particularly useful in high-frequency and impedance-matching applications.

5(b): Common-Source Amplifier - Gain Calculation:

Given Data

$g_m=3"\ mS"$

$R_D=12"\ k"\ \Omega$

$r_o=60"\ k"\ \Omega$

Step 1: Identify Effective Output Resistance

In a practical CS amplifier, the drain sees both the drain resistor $R_D$and the transistor output resistance r_o. Therefore,

$R_{out}=R_D \| r_o$

$R_{out}=(R_D \cdot r_o)/(R_D+r_o\ )$

$R_{out}=(12\times60)/(12+60)\ k\Omega$

$R_{out}=720/72$

$R_{out}=10\ k\Omega$

Step 2: Voltage Gain Calculation

Voltage gain of common-source amplifier:

$A_v=-g_m\ R_{out}$

Substituting values:

$A_v=-(0.003)(10000)$

$A_v=-30$

Step 3: Interpretation

->Negative sign indicates 180° phase inversion between input and output.

->Magnitude of gain = 30.

->Gain is limited by finite output resistance r_o.

If r_o were infinite, gain would be:

$A_v=-g_m R_D=-36$

Thus channel length modulation slightly reduces gain.

The common-source amplifier provides moderate voltage gain with phase inversion. Practical gain depends on both R_D and transistor output resistance, making device parameters crucial in analog CMOS design.

6(a): Effect of Non-Ideal Tail Current Source on CMRR:

A differential amplifier ideally amplifies only the difference between two input signals and rejects common-mode signals. However, in practical circuits, the tail current source is not ideal and has finite output resistance r_{tail}. This non-ideality directly affects Common Mode Rejection Ratio (CMRR).

1. Differential Gain

For a MOS differential pair with load resistance R_D:

$A_d=g_m R_D$

where g_m is transconductance of each transistor.

2. Common-Mode Gain

In ideal case, tail current source has infinite resistance, so common-mode gain A_{cm} is zero.

In practical case:

$A_{cm} \approx R_D/(2r_{tail})$

Since r_{tail} is finite, common-mode signals cause variations in tail current, producing unwanted output.

3. CMRR Expression

$CMRR = A_d/A_{cm}$

Substituting:

$CMRR \propto g_m r_{tail}$

Thus, higher tail resistance improves CMRR.

4. Design Implications

->Use cascoded current sources to increase r_{tail}.

->Increase channel length of current source transistor.

->Improve matching and bias stability.

Finite tail current source resistance introduces common-mode gain and reduces CMRR. High-performance differential amplifiers require large r_{tail} to achieve good noise rejection and precision.

6(b): Input Offset Voltage in Differential Amplifier :

Input offset voltage (V_{OS}) is the small differential input voltage required to make the output zero when ideally both inputs are equal. It arises due to mismatch between transistors in the differential pair.

1. Causes of Offset

->Threshold voltage mismatch (ΔV_T)

->Mobility mismatch

->Channel length/width variations

->Process variations

Among these, threshold mismatch is dominant.

2. Approximate Expression

For a differential pair:

$V_{OS} \approx \Delta V_T$

If threshold mismatch is ±6 mV, then:

$V_{OS} \approx 6$ mV

This means even when both inputs are equal, output will not be exactly zero.

3. Effect on Circuit Performance

->Reduces precision in op-amps

->Causes DC error in amplifiers

->Limits accuracy in instrumentation circuits

->Produces output offset voltage equal to:

$V_{(out,offset)} = A_d \times V_{OS}$

Even small input offset becomes large after amplification.

4. Methods to Reduce Offset

->Increase device area

->Use common-centroid layout

->Use chopping or auto-zero techniques

->Proper biasing

Input offset voltage is an important non-ideality caused mainly by device mismatch. Careful layout and design techniques are essential to minimize offset in precision analog circuits.

OR

7(a): Gilbert Cell Multiplier - Operation and Analysis :

The Gilbert cell is a widely used CMOS analog multiplier and mixer, especially in RF and communication circuits. It is a fully differential structure that performs signal multiplication using a transconductance stage followed by a switching quad.

1. Structure

A typical Gilbert cell consists of:

->Differential input pair (transconductance stage)

->Cross-coupled switching quad

->Load resistors or active loads

The lower differential pair converts input voltage into current, while the upper switching quad steers this current between outputs.

2. Principle of Operation

The drain current of a differential pair is:

$I_D = I_{tail} \tanh(V_{in}/(2V_T))$

The switching quad multiplies this current with another input signal.

Thus, output current becomes proportional to the product of two input signals: $I_{out} \propto V_{RF} \times V_{LO}$

This makes the Gilbert cell a four-quadrant multiplier.

3. Advantages

->Fully differential operation

->Good linearity

->High port isolation

->Even harmonic cancellation

->Suitable for high-frequency applications

4. Applications

->RF mixers

->Modulators and demodulators

->Balanced multipliers

->Frequency converters

The Gilbert cell efficiently performs analog multiplication using differential current steering. Its symmetry and differential architecture make it highly suitable for communication IC design.

7(b): Single-Ended vs Differential Output Comparison :

In analog circuits, outputs can be either single-ended or differential. The choice significantly affects performance parameters such as gain, noise rejection, and linearity.

1. Single-Ended Output

In single-ended configuration, output is taken from one node with respect to ground.

*Characteristics:

->Simpler design

->Lower power consumption

->Moderate gain

->More susceptible to noise

Since only one output node carries signal, common-mode noise directly affects output.

2. Differential Output

In differential configuration, output is taken between two nodes:

$V_{out}=V_{(out+)}-V_{(out-)}$

*Advantages:

->Higher effective gain

->Improved Common Mode Rejection Ratio (CMRR)

->Cancellation of even-order harmonics

->Better noise immunity

->Reduced distortion

->Differential signaling suppresses common-mode interference, making it ideal for precision and RF circuits.

3. Comparison

Parameter-> Single-Ended || Differential

Gain-> Lower || Higher

Noise immunity-> Poor || Excellent

Linearity-> Moderate || High

Power-> Lower || Slightly higher

While single-ended outputs are simpler and consume less power,

differential outputs offer superior gain, noise rejection, and linearity. Hence, differential architecture is preferred in high-performance analog and communication systems.

8(a): Simple Current Mirror vs Cascode Current Mirror:

Current mirrors are fundamental biasing blocks in CMOS analog circuits. They replicate a reference current I_REF to generate a stable output current I_O. The two commonly used configurations are the simple current mirror and the cascode current mirror.

1. Simple Current Mirror:

A basic current mirror consists of two matched MOS transistors. The gate and drain of the reference transistor are connected together to form a diode connection. Since both transistors share the same V_GS, ideally:

I_O=I_REF ((W/L_2)/(W/L_1))

If the devices are identical:

I_O=I_REF

*Advantages:

->Simple structure

->Low area

->Low compliance voltage

->Easy implementation

*Limitations:

->Low output resistance

->Affected by channel length modulation

->Poor accuracy in deep submicron technology

Output resistance is:

$r_o = 1/(\lambda I_D)$

Finite $r_o$causes output current to vary with V_{DS}.

2. Cascode Current Mirror

The cascode mirror improves performance by adding a second transistor in series. This increases output resistance significantly:

$r_{(o,eff)} \approx g_m r_o^2$

Higher output resistance improves current accuracy and reduces variation due to channel length modulation.

*Advantages:

->High output resistance

->Improved current accuracy

->Reduced dependence on output voltage

*Limitations:

->Higher compliance voltage

->Reduced output swing

->Larger area

The simple mirror is suitable for low-voltage and area-constrained designs, while the cascode mirror is preferred in precision analog circuits requiring high output resistance and better current stability.

8(b): Principle of Current Mirroring in MOSFETs :

Current mirroring in MOSFET circuits is based on the principle that two matched transistors operating with equal gate-to-source voltage V_{GS} will conduct proportional drain currents.

1. Basic Operating Principle:

For a MOSFET in saturation:

$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$

If two transistors share the same V_{GS} and are fabricated identically, their currents are proportional to their aspect ratios:

$I_O / I_{REF} = (W/L)_2 / (W/L)_1$

Thus, output current is:

$I_O = I_{REF} \left(\frac{(W/L)_2}{(W/L)_1} \right)$

2. Conditions for Accurate Mirroring:

->Transistors must operate in saturation

->Equal V_{GS}

->Good device matching

->Similar V_{DS}(to reduce channel length modulation errors)

3. Practical Considerations

Channel length modulation causes slight variation in output current:

$I_D = I_{ideal} (1 + \lambda V_{DS})$

Temperature variations and mismatch also affect accuracy.

4. Applications

->Bias current generation

->Active loads in amplifiers

->Reference current distribution

->Analog building blocks

Current mirroring is a fundamental technique for generating stable bias currents in CMOS circuits. Its accuracy depends on matching, saturation operation, and minimizing second-order effects such as channel length modulation.

OR

9(a): Passive vs Active Current Mirrors :

Current mirrors are essential building blocks in analog CMOS circuits. Based on implementation, they can be classified into passive current mirrors and active current mirrors. The performance, accuracy, and output resistance differ significantly between the two.

1. Passive Current Mirror:

A passive current mirror typically uses resistors to establish a current ratio. The output current is determined by Ohm's law:

I=V/R

*Characteristics:

->Simple structure

->No active device stacking

->Low design complexity

*Limitations:

->Poor current accuracy

->Strong dependence on supply voltage

->Large area due to resistor implementation

->Low output resistance

Since output current directly depends on resistor values and supply variations, precision is limited. Therefore, passive mirrors are rarely used in integrated CMOS analog circuits.

2. Active Current Mirror:

An active current mirror uses MOS transistors operating in saturation.

The output current is given by:

$I_O=I_{REF} ((W/L)_2/(W/L)_1)$

Because transistors operate in saturation, the output resistance is:

$r_o=1/(\lambda I_D)$

This provides significantly higher output resistance compared to passive mirrors.

*Advantages:

->High current accuracy

->High output resistance

->Better matching in IC fabrication

->Suitable for precision analog circuits

3. Comparison

Parameter->	Passive Mirror ||	Active Mirror
Accuracy->	Low ||	High
Output Resistance->	Low ||	High
Area->	Large ||	Compact
Supply Dependence->	High ||	Low

Active current mirrors are preferred in CMOS analog IC design due to superior accuracy, high output resistance, and better integration capability compared to passive implementations.

9(b): Current Mirror Numerical and Mirror Ratio :

In a MOS current mirror, output current is determined by transistor aspect ratio and reference current. The principle is based on equal gate-to-source voltage $V_{GS}$for matched devices operating in saturation.

Given

Reference current:

$I_{REF}=120\mu A$

Assume identical transistors:

$(W/L)_1=(W/L)_2$

Step 1: Current Ratio Formula

For MOSFET in saturation:

$I_D=1/2\ \mu C_{ox}\ W/L(V_{GS}-V_T)^2$

Since both transistors have same V_{GS}:

$I_O/I_{REF}=(W/L)_2/(W/L)_1$

Step 2: Substitute Values

If ratio = 1:

$I_O=I_{REF}$

$I_O=120\mu A$

Thus mirror ratio = 1:1.

Step 3: Practical Considerations

In real circuits, output current slightly varies due to:

->Channel length modulation

->Threshold mismatch

->Temperature variations

Including channel length modulation:

$I_D=I_{ideal}(1+\lambda V_{DS})$

This introduces slight error in output current.

For identical devices, the output current equals reference current (120 μA).

The mirror ratio is determined solely by transistor aspect ratios. Accurate current mirroring requires good matching and operation in saturation region.

10(a): Two-Stage CMOS Op-Amp - Gain Derivation :

A two-stage CMOS operational amplifier is widely used when high DC gain is required. It typically consists of a differential input stage followed by a common-source gain stage. The overall gain is the product of the gains of individual stages.

1. First Stage (Differential Amplifier)

The first stage converts differential input voltage into current and provides initial gain.

Small-signal gain:

$A_1=g_{m1}\, r_{o1}$

where

g_{m1}= transconductance of input transistor

r_{o1}= output resistance of first stage

This stage provides moderate gain and high input impedance.

2. Second Stage (Common-Source Amplifier)

The second stage further amplifies the signal.

$A_2 = g_{m2} r_{o2}$

where

g_{m2}= transconductance of second stage transistor

r_{o2}= output resistance

3. Overall DC Gain

Since stages are cascaded:

$A_v = A_1 \times A_2$

$A_v = (g_{m1} r_{o1})(g_{m2} r_{o2})$

Thus very high gain (60-80 dB or more) can be achieved.

4. Frequency Considerations

Two high-gain stages introduce two poles, reducing stability. Hence Miller compensation capacitor C_c is used to create a dominant pole:

$f_{p1} = 1/(2\pi R_1 C_c)$

This ensures adequate phase margin.

A two-stage op-amp achieves high voltage gain by cascading two amplifying stages. Proper compensation is essential to maintain stability while achieving high DC gain.

10(b) : Output Swing in Two-Stage CMOS Op-Amp :

Output swing refers to the maximum voltage range over which the

op-amp can operate without distortion while keeping all transistors in saturation.

1. Supply Conditions

Given supply voltages:

+3V"and"-3V

Total supply range = 6 V.

2. Saturation Requirement

For a MOSFET to remain in saturation:

$V_{DS} \geq V_{OV}$

Typically, a minimum voltage of about 0.5 V is required from each rail to maintain saturation.

3. Maximum Output Voltage

Upper limit:

$V_{(out(max))}=V_{DD}-V_{sat}$

$V_{(out(max))}=3-0.5=2.5V$

4. Minimum Output Voltage

Lower limit:

$V_{(out(min))}=-3+0.5=-2.5V$

5. Total Output Swing

Peak-to-peak swing:

$V_{pp}=2.5-(-2.5)=5V$

Thus maximum output swing is ±2.5 V.

6. Practical Considerations

Output swing depends on:

->Overdrive voltage

->Device stacking

->Cascode structures

->Supply voltage

Higher stacking reduces swing due to headroom limitation.

Output swing in a two-stage op-amp is limited by saturation constraints of output transistors. Proper biasing and minimizing device stacking help maximize available voltage swing.

OR

11(a): Effect of Load Capacitance on Amplifier Performance :

Load capacitance C_L plays a critical role in determining the frequency response and stability of CMOS amplifiers. It appears at the output node and directly influences bandwidth and phase margin.

1. Formation of Output Pole

In a common-source or op-amp output stage, the output resistance R_{out} combined with load capacitance forms a dominant pole:

$f_p=1/(2\pi R_{out} C_L)$

As C_L increases, the pole frequency decreases, thereby reducing bandwidth.

2. Effect on Bandwidth

Bandwidth is inversely proportional to load capacitance:

$BW\propto 1/C_L$

A large load capacitance slows down the response of the amplifier, increasing rise time and settling time. This limits speed performance in high-frequency circuits.

3. Effect on Stability

In multi-stage amplifiers, such as two-stage op-amps, load capacitance introduces additional poles. If these poles are not properly controlled using compensation techniques (e.g., Miller compensation), phase margin reduces, leading to:

->Overshoot

->Ringing

->Oscillation

Hence stability becomes a major concern when driving large capacitive loads.

4. Impact on Slew Rate

Slew rate is given by:

SR=I_bias/C_L

Larger C_L reduces slew rate, making output transitions slower.

Load capacitance reduces bandwidth, slows transient response, and can degrade stability. Proper compensation and adequate bias current are necessary to ensure stable and high-speed amplifier operation.

11(b): Gain Boosting Technique in CMOS Amplifiers:

Gain boosting is a technique used in CMOS analog circuits to increase output resistance and thereby improve voltage gain without significantly

increasing device stacking.

1. Need for Gain Boosting

The intrinsic gain of a MOS transistor is:

$A_v = g_m r_o$

In short-channel technologies, output resistance r_o decreases due to channel length modulation, limiting achievable gain.

2. Principle of Gain Boosting

In a cascode configuration, output resistance is already improved:

$r_{o,cascode} \approx g_m r_o^2$

Gain boosting further enhances this by adding an auxiliary amplifier to control the gate voltage of the cascode transistor.

Effective output resistance becomes:

$r_{o,eff} = A_{boost} \cdot r_o$

where A_{boost} is gain of the auxiliary amplifier.

3. Advantages

->Significantly increases DC gain

->Improves precision

->Reduces gain error

->Useful in high-performance op-amps

4. Limitations

->Increased circuit complexity

->Additional power consumption

->Reduced bandwidth

->Stability concerns

Gain boosting enhances effective output resistance and improves amplifier gain without excessive stacking. It is widely used in high-gain CMOS operational amplifiers, though careful compensation is required to maintain stability.