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CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–I–Semester End Examinations (Regular) - February- 2026
CMOS ANALOG IC DESIGN
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a)	How does body effect modify the threshold voltage of a MOSFET?	[2M]
b)	Why is the output voltage swing limited in a resistively loaded CS amplifier?	[2M]
c)	Define Common-Mode Rejection Ratio (CMRR) and state one factor that limits it.	[2M]
d)	What limits the minimum compliance voltage in a cascode current mirror?	[2M]
e)	How does gain boosting enhance op-amp performance?	[2M]

PART-B **(50 Marks)**

2.a)	Analyze the impact of velocity saturation on MOS I–V characteristics in short-channel devices.	[5M]
b)	An NMOS transistor operates in saturation with the following parameters: V_{GS}=3.5V, V_T=1V, K_n=250 μA/V^2, channel length modulation parameter λ=0.02 V^{-1}, and V_{DS}=5V. 1. Verify whether the transistor is in saturation. 2. Calculate the drain current including channel length modulation.	[5M]
	OR	
3.a)	Discuss the trade-offs involved in selecting MOS device models for precision analog design.	[5M]
b)	Explain why second-order effects are critical in scaled MOS technologies for analog circuits.	[5M]
4.a)	Analyze the frequency response of a common-gate amplifier and its suitability for high-frequency applications.	[5M]
b)	Evaluate the trade-offs between gain, bandwidth, and power consumption in single-stage amplifiers.	[5M]
	OR	
5.a)	Justify the use of common-gate amplifiers in low-input-impedance applications.	[5M]
b)	A common-source MOS amplifier uses a resistive load with the following parameters: g_m=3 mS, RD=12 kΩ, and output resistance r_o=60 kΩ. 1. Draw the small-signal equivalent circuit. 2. Calculate the voltage gain of the amplifier.	[5M]
6.a)	Evaluate the effect of tail current source non-idealities on CMRR.	[5M]
b)	A differential amplifier exhibits a threshold voltage mismatch of ±6 mV and transconductance of 4 mS. Estimate the input offset voltage.	[5M]
	OR	
7.a)	Explain the working principle of a Gilbert cell and its applications.	[5M]
b)	Compare single-ended and differential outputs in MOS differential amplifiers.	[5M]

8.a)	Evaluate the trade-offs between simple and cascode current mirrors.	[5M]
b)	Explain the basic principle of current mirroring in MOS circuits.	[5M]
	OR	
9.a)	Compare passive current mirrors and active current mirrors in analog IC design.	[5M]
b)	A basic MOS current mirror has a reference current of 120 μA. Assuming ideal matching, calculate the output current and mirror ratio.	[5M]
10.a)	Derive the gain expression of a two-stage CMOS operational amplifier.	[5M]
b)	A two-stage CMOS operational amplifier operates from ±3 V supplies. If the minimum output saturation voltage is 0.5 V from each supply rail, determine the maximum output voltage swing.	[5M]
	OR	
11.a)	Analyze the effect of load capacitance on op-amp stability.	[5M]
b)	Analyze the role of gain boosting in improving DC gain.	[5M]

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