Code No.: R25EC57101PC | R25 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–I–Semester End Examinations (Regular) - February- 2026
CMOS DIGITAL IC DESIGN
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a)	Compare static and dynamic behavior of CMOS inverter.	[2M]
b)	List out the phases of dynamic CMOS logic.	[2M]
c)	Recall the bistability principle in static latches.	[2M]
d)	State advantages of gate arrays.	[2M]
e)	Define cross talk.	[2M]

PART-B **(50 Marks)**

2.a)	Draw and explain the voltage transfer characteristics of a CMOS inverter.	[5M]
b)	Analyze the dynamic characteristics of a CMOS inverter	[5M]
	OR	
3.	Develop a methodology to minimize energy-delay product in CMOS inverter design.	[10M]
4.a)	Illustrate the operation of pass transistor logic with example.	[5M]
b)	Summarize the need for reduced supply voltage logic design.	[5M]
	OR	
5.	Examine the issues in dynamic logic design such as charge sharing and clock feed-through.	[10M]
6.	Evaluate a master-slave flip-flop using CMOS logic.	[10M]
	OR	
7.	Develop a pipelined architecture using latch-based design and evaluate its throughput.	[10M]
8.	Analyze the complete flow of cell-based ASIC design methodology.	[10M]
	OR	
9.	Explain different implementation strategies used in digital IC design.	[10M]
10.	Explain the concept of reduced-swing circuits in advanced interconnect approaches.	[10M]
	OR	
11.	Analyze the impact of resistive parasitic on reliability and performance with neat diagrams.	[10M]

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I M.Tech - I. Semester End Examinations

CMOS DIGITAL IC DESIGN

(VLSI SD)

Total mark: (60m)

PART-A

1(a) Comperison static and dynamic behavior of cmos Inverter.

Parameter	Static Behavior	Dynamic Behavior
Condition	De steady i/p	Switching condition
Analysis Tool	VTC Curve	Transcient
Power dissipation	Ideally Zero	Significant

Static Behavior determines reliability and noise immunity

Dynamic behavior determines speed and power consumption —— (2m)

b) list out the phases of dynamic cmos logic

Precharge phase (CLK=0)

Evaluation phase (CLK=1) —— (2m)

c) The Bistability principle in static latches.

→ Based on positive feedback.
→ Two stable state Q=1 or Q=0
Implemented using cross coupled Inverters.
→ Once set, o/p remains stable until i/p changes (2m)

d) Gate arrays offer a semi custom ASIC approach and faster time-to-market compared to full custom design.

→ ~~(Reduced)~~ Faster turnaround time.
→ Prefabricated transistor arrays. (2m)

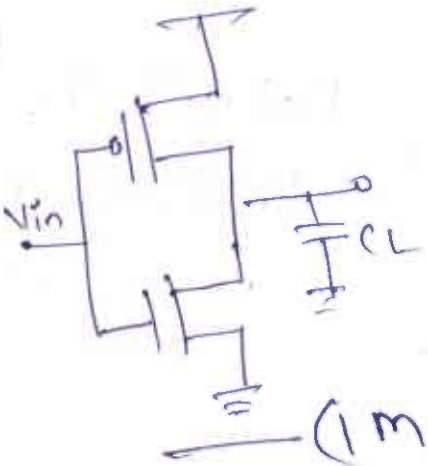
e) Cross talk:- Unwanted signal coupling b/n adjacent interconnects.

- Caused by capacitive and inductive coupling
- Leads to noise, delay variation and logic Errors. (2m)

PART-B

2(a) The voltage Transfer Characteristics of a CMOS inverter the relationship b/n the Vin and Vout

The VTC curve is divided into five distinct regions based on the operation modes on NMOS and PMOS transistors.



(1M)

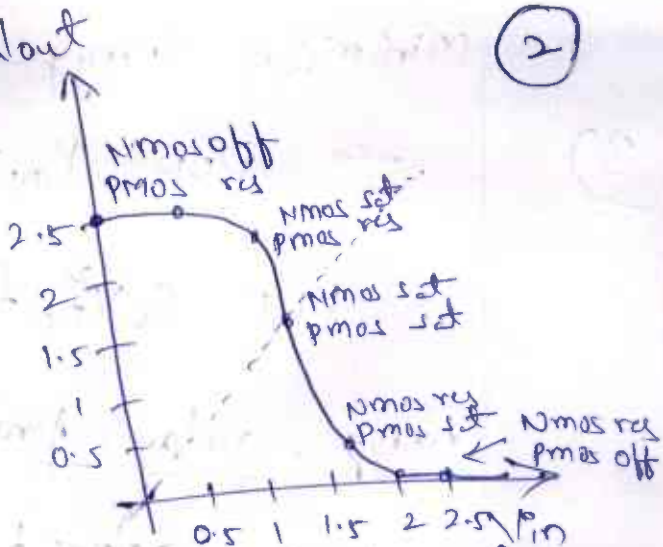
Region 1 ($0 < V_{in} < V_{tn}$)

Region 2 ($V_{tn} \leq V_{in} < V_m$)

Region 3 ($V_{in} = V_m$)

Region 4 ($V_m < V_{in} \leq V_{DD} - |V_{tp}|$)

Region 5 ($V_{in} > V_{DD} - |V_{tp}|$).



(2m)

(2m)

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b) CMOS inverters exhibit dynamic characteristics during input transitions, including propagation delay, rise/fall times and power dissipation from switching and short circuit currents. (1m)

Propagation delay $t_{PHL} = 0.69 R_n C_L$

$t_{PLH} = 0.69 R_p C_L$

Total delay $t_p = \frac{t_{PHL} + t_{PLH}}{2}$ (1m)

Rise and Fall time

Rise time $t_r = 2.2 R_p C_L$

$t_f = 2.2 R_n C_L$ (1m)

Power dissipation :-

$P = \alpha C_L V_{DD}^2 f + P_{sc} + P_{leak}$. (2m)

3) Minimize Energy-delay product in CMOS.

→ $PDP = P_{av} t_p$ → PDP presents a measure of energy.

$$PDP = C_L V_{DD}^2 f_{max} t_p = \frac{C_L V_{DD}^2}{2}$$ —— (2m)

Energy - Delay product :-

$$EDP = PDP \times t_p = P_{av} t_p^2 = \frac{C_L V_{DD}^2}{2} t_p.$$

$$t_p \approx \frac{\alpha C_L V_{DD}}{V_{DD} - V_{TE}}.$$

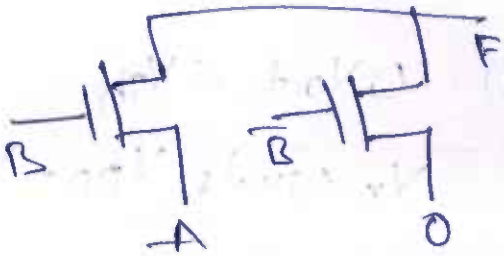
$$EDP = \frac{\alpha C_L^2 V_{DD}^3}{2(V_{DD} - V_{TE})}$$

$$\boxed{V_{DDopt} = \frac{3}{2} V_{TE}}$$ —— (4m)

Optimization methodology

→ transistor sizing
→ logical effort minimization
→ Reduce V_{DD} carefully
→ Buffer Insertion for long wires
→ Use multi Vt devices
→ Reduce parasitic capacitance
→ Technology scaling. —— (4m)

4(a) Pass transistor logic :- PTL Uses MOSFETS as switches to pass input signals directly to o/p based on control gates, reducing transistor count Compared to static cmos. (3)



AND function Constructed Using only NMOS transistors. Pass transistor AND In this gate ; if the B input is high, the top transistor is turned on and copies the input A to the o/p F. - when B is low, the bottom pass transistor is turned on and passes a 0. — (3m)

Adv :- lower area, power ; good for multipleners,

limitation :- Threshold drop degrades signal, more leakage paths. — (2m)

4b) Reduced Supply voltage logic design addresses escalating power demands in modern cmos circuits by minimizing dynamic and leakage power consumption.

(i) Reduction in Dynamic Power Consumption

$$P = \alpha C_L V_{DD}^2 f.$$

(ii) Essential for portable and Battery Operated

(iii) Reduced Heat Generation

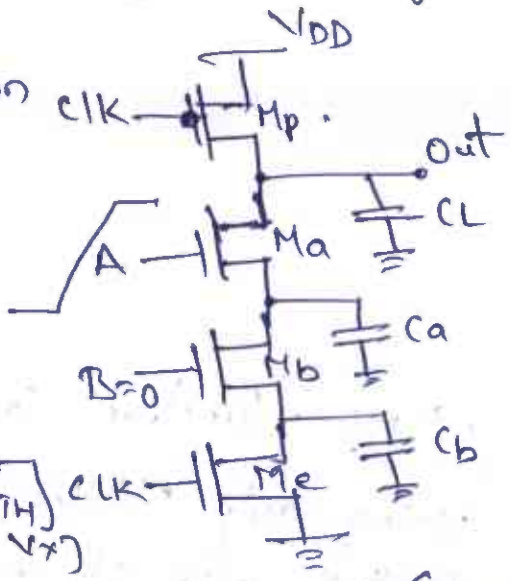
(iv) Improved Device Reliability

(v) Technology Scaling Compatibility

— (5m)

5) Important Concern in dynamic logic is charge sharing:

During the precharge/evaluation phases.



(1) $\Delta V_{out} < V_{Th}$

V_x equals $V_{DD} - V_{Th}(V_x)$

$C_L V_{DD} = C_L V_{out} + C_a [V_{DD} - V_{TH}(V_x)]$

$\Delta V_{out} = V_{out}(final) + (-V_{DD}) = -\frac{C_a}{C_L}[V_{DD} - V_{Th}(V_x)]$ ——— (3m)

(2) $\Delta V_{out} > V_{Th}$. $\Delta V_{out} = -V_{DD}\left(\frac{C_a}{C_a + C_L}\right)$

$$\frac{C_a}{C_L} = \frac{V_{Th}}{V_{DD} - V_{Th}}$$

——— (3m)

Clock Feedthrough :- Clock-feedthrough arises from capacitive coupling (C_{gd}, C_{gs}) b/n clock and o/p nodes, injecting charge via miller effect during fast CLK edges. This causes unwanted voltage spikes on the dynamic node (50-200mV), worsend by fast clock slew rates and large clock transistor overlap capacitances.

——— (4m)

6) Master slave Flip flop using cmos logic :- provide edge triggered storage by isolating input (master) and output (slave) stages with complementary clock signals, preventing race conditions in sequential circuits. — (2m)

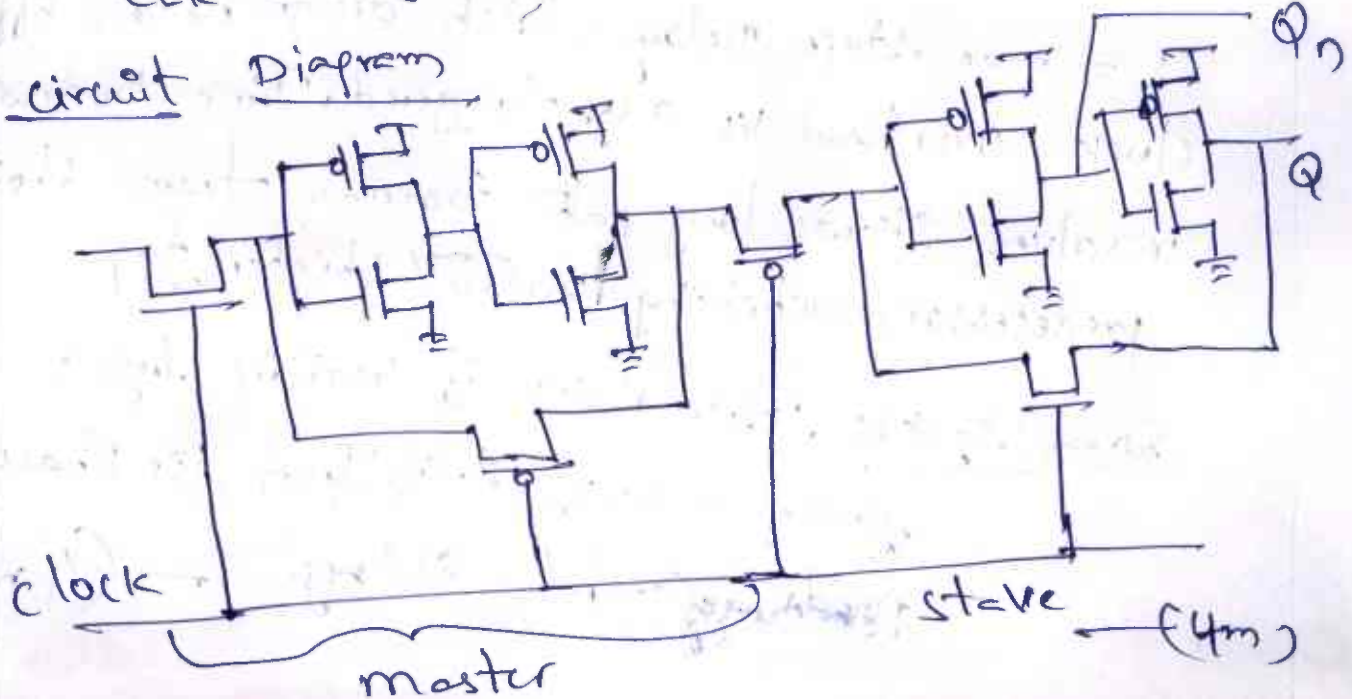
cmos Implementation :-

Transmission gate based design uses two latches : master (transparent when CLK=0 via TG1 and ON and TG2 OFF) captures D; slave transparent drives Q. Each latch comprises cross coupled inverters. for state hold and transmission gates — (2m)

Operation phases :-

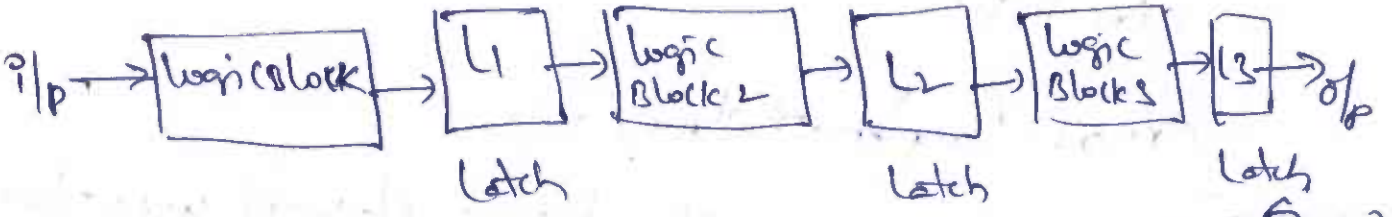
CLK low :- master samples D
CLK RISING EDGE :- master latches value, slave
CLK high : slave tracks master's
CLK falling : slave latches — (2m)

Circuit Diagram



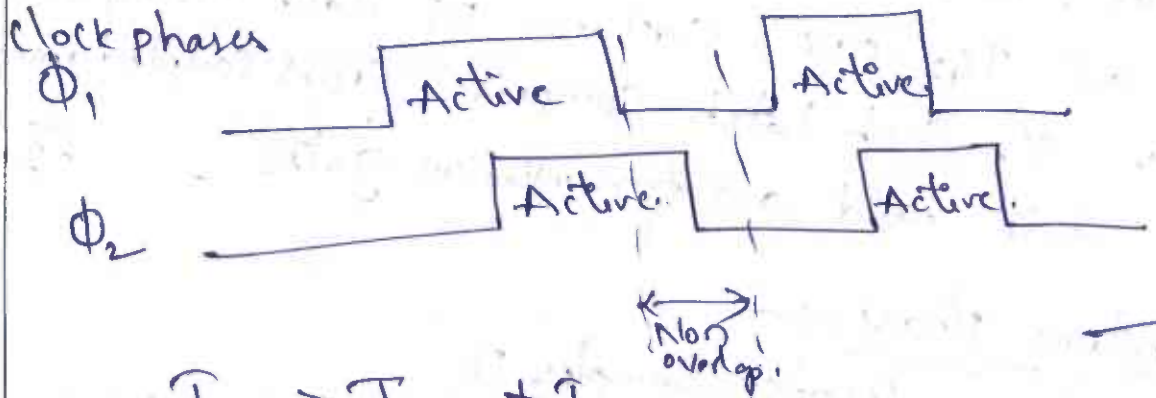
— (4m)

7) Latch Based Pipelined architecture use level Sensitive latches arranged in alternating phases to enable time borrowing, improving, throughput over flipflop registers.



(3m)

Two phases clock Signals (Non overlapping)



(3m)

$T_{CLK} \geq T_{logic} + T_{non\ overlap}$.

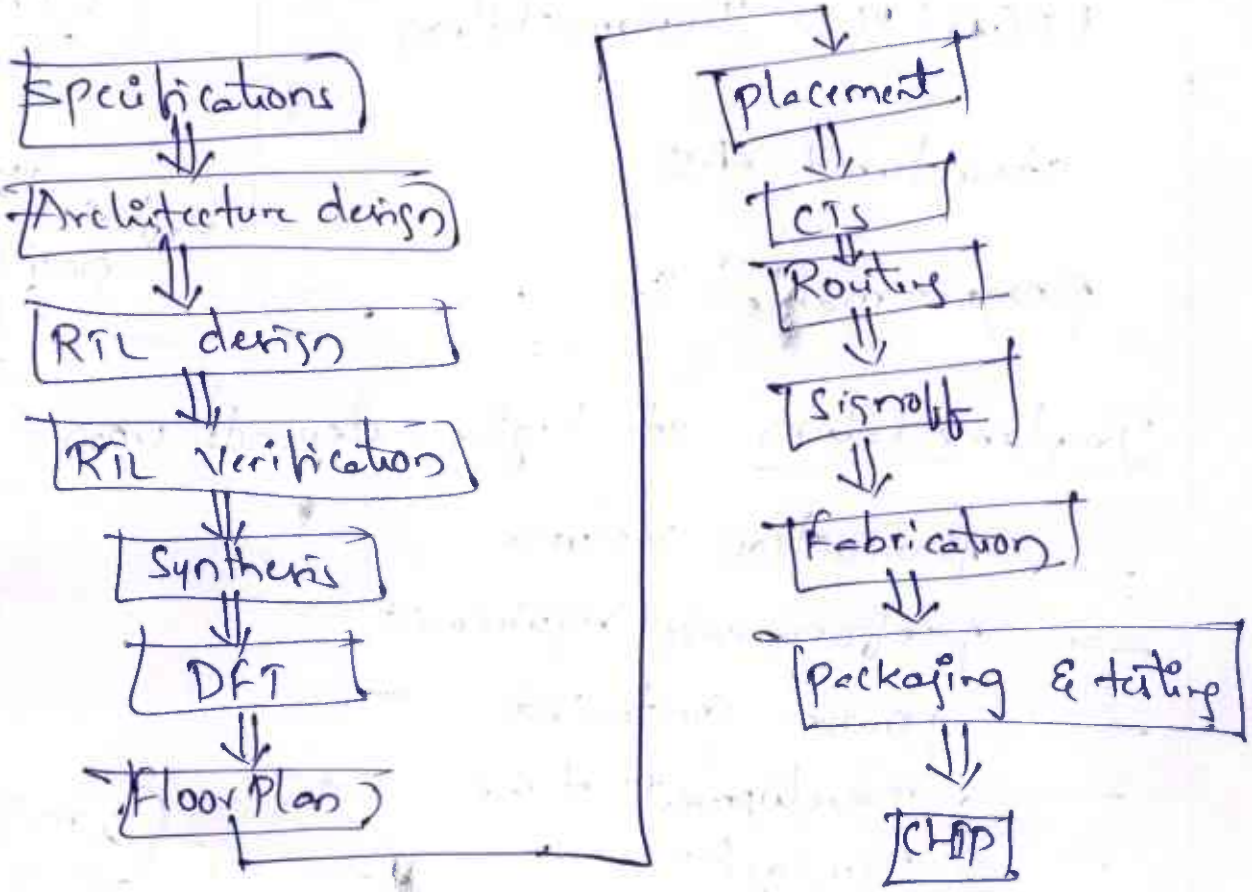
Through put Evaluation :- Throughput $= \frac{1}{T}$,

T = max stage Delay; latch design halves Effective clock overhead Vs edge triggered. Time borrowing resolves skew; long path borrows from short predecessor, achieving 20-50% higher freq

Drawbacks: Race risks if inverting logic;
power ~ 50% utilization per phase.
needs careful sizing. —(4m)

8) Complete flow of Cell Based ASIC design methodology :-

Cell Based ASIC Design flows translate functional specifications into physical chips (RTL to GDSII). Using pre designed, standard logic cells.
The methodology consists of a front end logical design (Specification, HDL coding, Synthesis) and back end physical design (floor planning, placement, clock tree Synthesis, routing and verification) — (2m)



Explanations with RTL Explanations (8m)

9) DIGITAL IC Design Employs multiple implement-tion strategies balancing performance, cost, time to market, and flexibility, ranging from fully Custom to programmable approaches. — (2m)

Full custom Design:-

Standard Cell Based Design

Gate array

FPGA/PLD Implementation

Structured ASIC

Programmable SoC

Brief Explanation (6m)

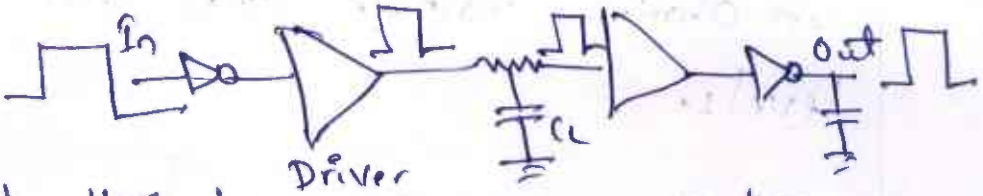
Explain the Design Flow — (6m)

Implementation strategies depends upon

- production volume
- performance requirement
- power constraint
- Development time
- Budget

— (2m)

10 Reduced Swing circuits in advanced interconnect



Increasing size of the driver transistor and thus increasing the average current I_{av} during switching is only one way of coping with the delay caused by a large load capacitance

$$t_p = \int_{V_1}^{V_2} \frac{C_L(V)}{i(V)}\, dv.$$

$$t_p = \frac{C_L V_{swing}}{I_{av}}.$$

(6m) (with explanation)

Core Concept:- Long Interconnect (wires > 100 μm) dominate delay ($RC \propto L^2$) and dynamic power ($P \propto CV^2f$) in deep Submicron designs. Reduced swing drives o/p $V_{swing} < V_{DD}$ having charging energy on wire capacitance while receiver use differential amplifiers. — (2m)

Driver Recivers pair:-

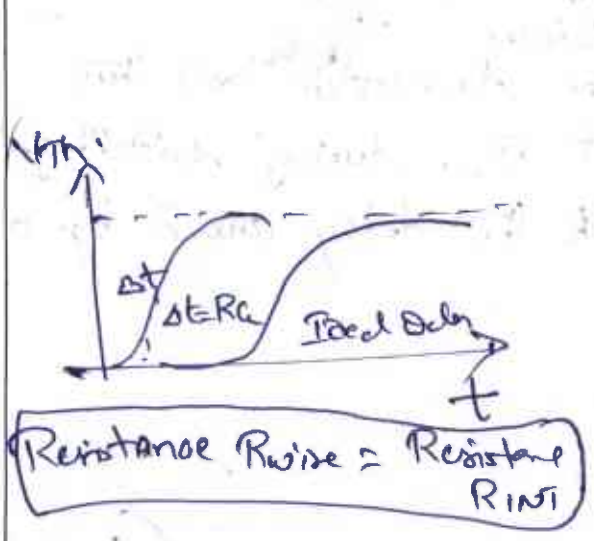
Pmos current Source charges wire to $V_{low} < V_{DD}$

$V_{low} = V_{DD} - V_{drop}$; Nmos pulls to high $\geq V_{tn}$.

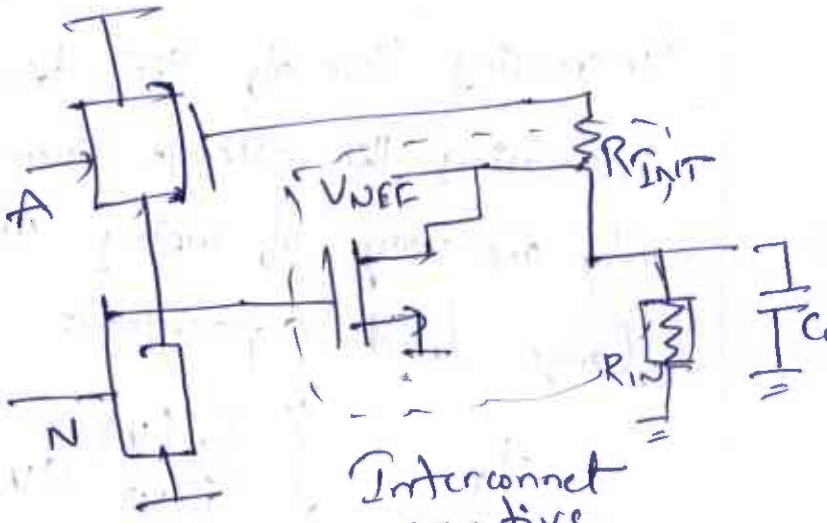
Reciver:- Cross Coupled Sense amp detects small differential. Source follower restores full swing. — (2m)

11) Resistive parasitics :-

Current flowing through a resistive wire results in an ohmic voltage drop that degrades the signal levels.



Resistance Rwire = Resistance R_{INT}



Interconnect resistive parasitics

Impact of resistive parasitics — (4m)

→ Increase Signal Delay RC Delay ↑
→ Heat Generation
→ Increased voltage Drop
→ Decreased Signal Integrity — (2m)

Corrective measures

— Use wider metal layer.
— Insert Additional Buffers.
— Optimize Interconnect Layout

— Signoff :- Increased Resistance
—Insert Additional Buffers (4m)
— Use low Resistance material.

Increased Resistance (R_{INT}) → Degrades performance & Reliability