

**CMR ENGINEERING COLLEGE: : HYDERABAD  
UGC AUTONOMOUS**

**I–M.TECH–I–Semester End Examinations (Regular) - February- 2026**

**CMOS DIGITAL IC DESIGN  
(VLSI SD)**

**[Time: 3 Hours]**

**[Max. Marks: 60]**

**Note:** This question paper contains two parts A and B.

Part A is compulsory which carries 10 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

**PART-A**

**(10 Marks)**

1. a) Compare static and dynamic behavior of CMOS inverter. [2M]
- b) List out the phases of dynamic CMOS logic. [2M]
- c) Recall the bistability principle in static latches. [2M]
- d) State advantages of gate arrays. [2M]
- e) Define cross talk. [2M]

**PART-B**

**(50 Marks)**

- 2.a) Draw and explain the voltage transfer characteristics of a CMOS inverter. [5M]
- b) Analyze the dynamic characteristics of a CMOS inverter [5M]

**OR**

3. Develop a methodology to minimize energy-delay product in CMOS inverter design. [10M]

- 4.a) Illustrate the operation of pass transistor logic with example. [5M]
- b) Summarize the need for reduced supply voltage logic design. [5M]

**OR**

5. Examine the issues in dynamic logic design such as charge sharing and clock feed-through. [10M]

6. Evaluate a master-slave flip-flop using CMOS logic. [10M]

**OR**

7. Develop a pipelined architecture using latch-based design and evaluate its throughput. [10M]

8. Analyze the complete flow of cell-based ASIC design methodology. [10M]

**OR**

9. Explain different implementation strategies used in digital IC design. [10M]

10. Explain the concept of reduced-swing circuits in advanced interconnect approaches. [10M]

**OR**

11. Analyze the impact of resistive parasitic on reliability and performance with neat diagrams. [10M]

\*\*\*\*\*