I M.Tech I Semester End Examinations (Regular) Feb-2026

Device modeling (R25EC57111PE)

PART A

1. **(a) Scaling and its benefits:**

Scaling refers to proportional reduction of MOSFET dimensions (L, W, tox) and voltages to improve device density and performance.

Benefits:

- Increased packing density
- Higher speed (reduced delay)
- Lower power per function
- Reduced cost per chip
- Improved frequency response

1(b) Narrow width effect:

Narrow width effect occurs when threshold voltage increases as channel width decreases due to lateral depletion encroachment and fringing fields from isolation regions.

1(c) Mobility degradation:

Mobility degradation refers to reduction in carrier mobility at high vertical electric fields due to surface scattering and phonon scattering, reducing drain current.

1(d) Hot-carrier degradation:

Hot carrier degradation occurs when high-energy carriers near drain gain sufficient energy to create interface traps or get injected into oxide, shifting threshold voltage and degrading gm.

1(e) Threshold voltage extraction methods:

Two methods:

1. Constant current method – Vth defined at specified drain current (e.g., ID = 1μA × W/L).
2. Linear extrapolation method – Extrapolate linear region ID–VGS curve to ID=0 to obtain V_{th}.

PART B

2. **Impact of Scaling Effects on Device Performance**

   1. **Short Channel Effects (SCE)**
      As channel length reduces, gate control weakens.
      - **DIBL (Drain Induced Barrier Lowering):** High drain voltage lowers the source-channel barrier, reducing threshold voltage.
      - **Vth Roll-off:** Threshold voltage decreases with reduced channel length.
      - Results in higher off-state current and poor control.
   2. **Increased Leakage Currents**
      Scaling increases various leakage components:
      - Subthreshold leakage
      - Gate oxide tunneling leakage
      - Junction leakage
        Leakage increases static power consumption significantly.
   3. **Velocity Saturation**
      At high electric fields (short channels), carriers reach saturation velocity.
      - Drain current becomes less dependent on gate voltage.
      - Reduces current drive compared to long-channel quadratic behavior.
      - Limits performance improvement from scaling.

4. **Mobility Degradation**
   High vertical electric field near the oxide interface causes:
   - Surface scattering
   - Phonon scattering
     This reduces effective mobility and hence drain current.
5. **Increased Variability**
   Device scaling increases:
   - Random dopant fluctuations (RDF)
   - Line-edge roughness (LER)
   - Oxide thickness variations
     This causes threshold voltage variation and mismatch in circuits.
6. **Higher Electric Fields and Reliability Issues**
   High fields cause:
   - Hot carrier degradation
   - Oxide breakdown (TDDB)
   - Bias Temperature Instability (BTI)
     Device lifetime reduces.

7. **Reduced Intrinsic Delay but Increased Parasitics**
   - Channel length reduction decreases intrinsic transit time → faster switching.
   - However, parasitic resistance and capacitance become comparable to intrinsic values.
   - Interconnect delay dominates at advanced nodes.

3. **(a) Parasitic capacitances in MOSFET:**

- Gate oxide capacitance (Cox)
- Overlap capacitances (Cgs, Cgd overlap)
- Junction capacitances (Cdb, Csb)
- Fringing capacitances
- Depletion capacitances

Parasitic Capacitances in MOSFET

In practical MOSFETs, several capacitances exist due to device structure and junctions. These affect switching speed and frequency response.

1. Gate Oxide Capacitance (Cox)

- Formed between gate and channel through thin oxide.
- Given by:

Cox=εoxtox×WLC_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \times WLCox=toxεox×WL
Where:

- εox\varepsilon_{ox}εox = permittivity of oxide
- toxt_{ox}tox = oxide thickness
- W,LW, LW,L = device dimensions

It is the **main controlling capacitance** of the MOSFET.

2. Overlap Capacitances (Cgs, Cgd overlap)

- Due to physical overlap of gate over source and drain regions.
- Independent of bias.
- Important in short-channel devices.

- Cgd contributes to **Miller effect**, increasing switching delay.

3. Junction Capacitances (Cdb, Csb)

- Due to reverse-biased PN junctions between:
  - Drain–body (Cdb)
  - Source–body (Csb)
- Voltage dependent.
- Given by:

Cj=Cj0(1+VR/ϕ0)mC_j = \frac{C_{j0}}{(1 + V_R/\phi_0)^m}Cj=(1+VR/ϕ0)mCj0

Where:

- VRV_RVR = reverse bias voltage
- mmm = grading coefficient

4. Fringing Capacitances

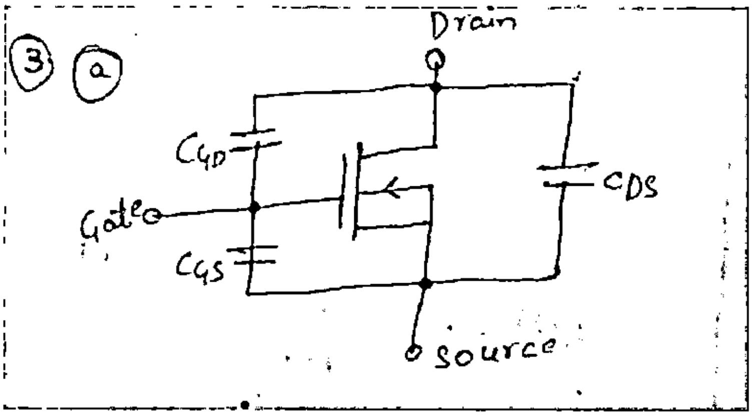
- Caused by electric field lines spreading from gate edges to source/drain.
- Significant in deep submicron devices.
- Increase total gate capacitance.

5. Depletion Capacitance

- Appears when device operates in depletion.
- Due to depletion region under gate.
- In series with oxide capacitance in depletion region.

Importance in VLSI

- Determine switching delay:
  td∝RCt_d \proptoRCtd∝RC
- Affect high-frequency performance.
- Critical in small-signal modeling.
- Dominant in scaled technologies.



3. (b) Modern multi-gate MOSFET structures:

Modern Multi-Gate MOSFET Structures

As planar MOSFET scaling faced severe short-channel effects (SCE), multi-gate devices were introduced to improve electrostatic control.

1. FinFET (Fin Field Effect Transistor)

- The channel is formed in a thin vertical silicon **fin**.

- The gate wraps around the fin on **three sides.**
- Provides better control of channel potential than planar MOSFET.

Key Features:

- Reduced DIBL
- Lower leakage current
- Higher drive current per footprint
- Used in advanced technology nodes (16nm, 7nm, 5nm)

2. Tri-Gate Structure

- A type of FinFET.
- Gate controls channel from **three sides** (left, right, top).
- Improves gate-channel coupling.
- Reduces threshold voltage roll-off.

3. Gate-All-Around (GAA) Nanowire FET

- Gate completely surrounds the channel (360° control).
- Channel formed as nanowire or nanosheet.
- Best electrostatic integrity among all structures.

Variants:

- Nanowire FET
- Nanosheet FET (used in sub-5nm nodes)

Advantages of Multi-Gate Devices

1. **Better Electrostatic Control**
    - Strong gate control over channel.
    - Reduced drain influence.
2. **Reduced Short Channel Effects (SCE)**
    - Lower DIBL
    - Reduced Vth roll-off
    - Suppressed punch-through
3. **Improved Subthreshold Slope**
    - Closer to ideal value (≈ 60 mV/dec at room temperature)
    - Lower off-state leakage
4. **Higher Drive Current**
    - Multiple channels increase effective width.
5. **Better Scalability**
    - Suitable for deep submicron technologies.

Conclusion

Multi-gate MOSFETs (FinFET, Tri-gate, GAA) are essential for advanced VLSI scaling because they provide superior channel control, lower leakage, and improved performance compared to planar MOSFETs.

4. (a) Flat-band and threshold voltage:

1. Flat-Band Voltage (VFB)

Flat-band condition occurs when **energy bands in semiconductor are flat**, i.e., no band bending and no space charge in semiconductor.

$VFB = \Phi MS - Qox/Cox$

Where:

- ΦMS=ΦM−ΦS\Phi_{MS} = \Phi_M - \Phi_SΦMS=ΦM−ΦS
  (Work function difference between metal and semiconductor)
- QoxQ_{ox}Qox = oxide charge density
- Cox=εoxtoxC_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}Cox=toxεox

Interpretation:

- If Qox=0Q_{ox} = 0Qox=0, then VFB=ΦMSV_{FB} = \Phi_{MS}VFB=ΦMS
- Positive oxide charge shifts VFBV_{FB}VFB negatively.
- It determines the starting point of C–V curve

Threshold Voltage (Vth)

Threshold voltage is the gate voltage at which **strong inversion** occurs.

Strong inversion condition:

ψs=2ΦF\psi_s = 2\Phi_Fψs=2ΦF

Where surface potential equals twice the Fermi potential.

Step 1: Fermi Potential

ΦF=kTqln(NAni)\Phi_F = \frac{kT}{q} \ln \left(\frac{N_A}{n_i}\right)ΦF=qkTln(niNA)

Where:

- NAN_ANA = substrate doping
- nin_ini = intrinsic carrier concentration

Step 2: Depletion Charge at Threshold

Maximum depletion charge:

Qd(max)=2εsiqNA(2ΦF)Q_{d(max)} = \sqrt{2 \varepsilon_{si} q N_A (2\Phi_F)}Qd(max)=2εsiqNA(2ΦF)

Step 3: Threshold Voltage Expression

Vth=VFB+2ΦF+Qd(max)CoxV_{th} = V_{FB} + 2\Phi_F + \frac{Q_{d(max)}}{C_{ox}}Vth=VFB+2ΦF+CoxQd(max)

Substituting:

Vth=VFB+2ΦF+2εsiqNA(2ΦF)CoxV_{th} = V_{FB} + 2\Phi_F + \frac{\sqrt{2 \varepsilon_{si} q N_A (2\Phi_F)}}{C_{ox}}Vth=VFB+2ΦF+Cox2εsiqNA(2ΦF)

Vth = VFB + 2ΦF + (√(2εsi q NA 2ΦF))/Cox

Where ΦF is Fermi potential, NA is substrate doping.

4. **(b) C–V characteristics:**

C–V Characteristics of MOS Capacitor

The capacitance–voltage (C–V) characteristics describe how the MOS capacitor behaves under different gate bias conditions.

1. Low-Frequency C–V Characteristics

At low frequency (≈ quasi-static condition), minority carriers can respond to the AC signal.

(a) Accumulation Region

- Gate voltage negative (for p-type substrate).
- Majority carriers (holes) accumulate at oxide interface.
- Capacitance ≈ Oxide capacitance.

C≈CoxC \approx C_{ox}C≈Cox

(b) Depletion Region

- Small positive gate voltage.
- Holes are repelled; depletion region forms.
- Capacitance is series combination of oxide and depletion capacitance:

C=CoxCdCox+CdC = \frac{C_{ox} C_d}{C_{ox} + C_d}C=Cox+CdCoxCd

- Capacitance decreases as depletion width increases.

(c) Inversion Region

- Large positive gate voltage.
- Strong inversion layer (electrons) forms.
- At low frequency, minority carriers follow AC signal.
- Capacitance increases back to:

C≈CoxC \approx C_{ox}C≈Cox

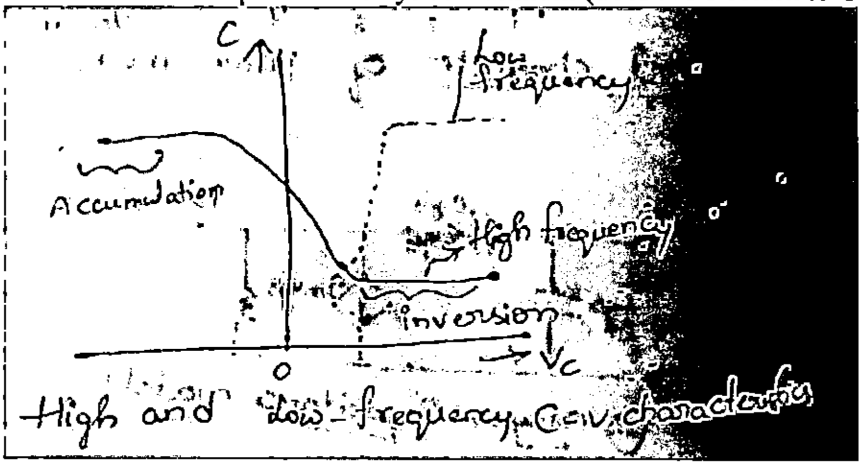
2. High-Frequency C–V Characteristics

At high frequency (≈ 1 MHz):

- Minority carriers cannot respond quickly.
- In inversion region, depletion width remains maximum.
- Capacitance remains at minimum value.

Behavior:

- Accumulation → C≈CoxC \approx C_{ox}C≈Cox
- Depletion → Capacitance decreases
- Inversion → Capacitance stays at minimum (does NOT return to Cox



High and Low frequency C-V characteristics

5(a) DIBL and channel length modulation:

1. DIBL (Drain Induced Barrier Lowering)

Definition:

DIBL is a short-channel effect where a **high drain voltage reduces the source-channel potential barrier**, effectively lowering the threshold voltage.

Physical Explanation:

- In short-channel MOSFETs, drain electric field extends toward the source.
- When VDSV_{DS}VDS increases:
    - Drain depletion region widens.

    - Source barrier height reduces.
    - Threshold voltage decreases.

Vth↓ as VDS↑V_{th} \downarrow \text{ as } V_{DS} \uparrowVth↓ as VDS↑

Effects:

- Increased off-state current (Ioff)
- Reduced gate control
- Higher leakage power
- Degraded subthreshold slope

DIBL Coefficient:

DIBL=ΔVthΔVDS\text{DIBL} = \frac{\Delta V_{th}}{\Delta V_{DS}}DIBL=ΔVDSΔVth

Measured in mV/V.

2. Channel Length Modulation (CLM)

Definition:

Channel Length Modulation is the reduction of **effective channel length** in saturation region as VDSV_{DS}VDS increases.

Physical Explanation:

- In saturation, pinch-off occurs near drain.
- Increasing VDSV_{DS}VDS:
    - Drain depletion region extends further into channel.
    - Effective channel length decreases.
    - Drain current increases slightly.

Modified Saturation Current Equation:

ID=12μCoxWL(VGS−Vth)2(1+λVDS)I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})ID=21μCoxLW(VGS−Vth)2(1+λVDS)

Where:

- λ\lambdaλ = Channel length modulation parameter

Effects:

- Non-zero output conductance
- Finite output resistance:

ro=1λIDr_o = \frac{1}{\lambda I_D}ro=λID1

- Reduced intrinsic gain in analog circuits

5(b) Short channel effects:

•. Short Channel Effects and Temperature Impact

As MOSFET channel length decreases, several non-ideal effects degrade performance.

1. Threshold Voltage Roll-Off

Definition:

Reduction in threshold voltage VthV_{th}Vth as channel length decreases.

Reason:

- Drain and source depletion regions extend into channel.
- Gate loses full control over channel charge.

Effect:

L↓⇒Vth↓L \downarrow \Rightarrow V_{th} \downarrowL↓⇒Vth↓

- Increases off-state leakage.
- Reduces noise margin in digital circuits.

2. DIBL (Drain Induced Barrier Lowering)

- High VDSV_{DS}VDS lowers source-channel barrier.
- Threshold voltage reduces with increasing drain voltage.

Vth↓ as VDS↑V_{th} \downarrow \text{ as } V_{DS} \uparrowVth↓ as VDS↑

Impact:

- Increased off-current (Ioff)
- Higher static power dissipation

3. Punch-Through

Definition:

Occurs when drain and source depletion regions merge.

Reason:

- Very short channel.
- High drain voltage.

Result:

- Current flows even without strong inversion.
- Device loses gate control.

4. Increased Subthreshold Leakage

In short-channel devices:

- Barrier lowering
- Reduced threshold voltage
- Thinner oxide

Cause exponential increase in:

Isub∝eVGSnVTI_{sub} \propto e^{\frac{V_{GS}}{nV_T}}Isub∝enVTVGS

Consequence:

- High standby power
- Thermal issues in VLSI chips

5. Temperature Effects

(a) Leakage Increases with Temperature

- Intrinsic carrier concentration increases.
- Subthreshold leakage increases exponentially.

ni∝e−Eg/2kTn_i \propto e^{-E_g/2kT}ni∝e−Eg/2kT

(b) Mobility Decreases with Temperature

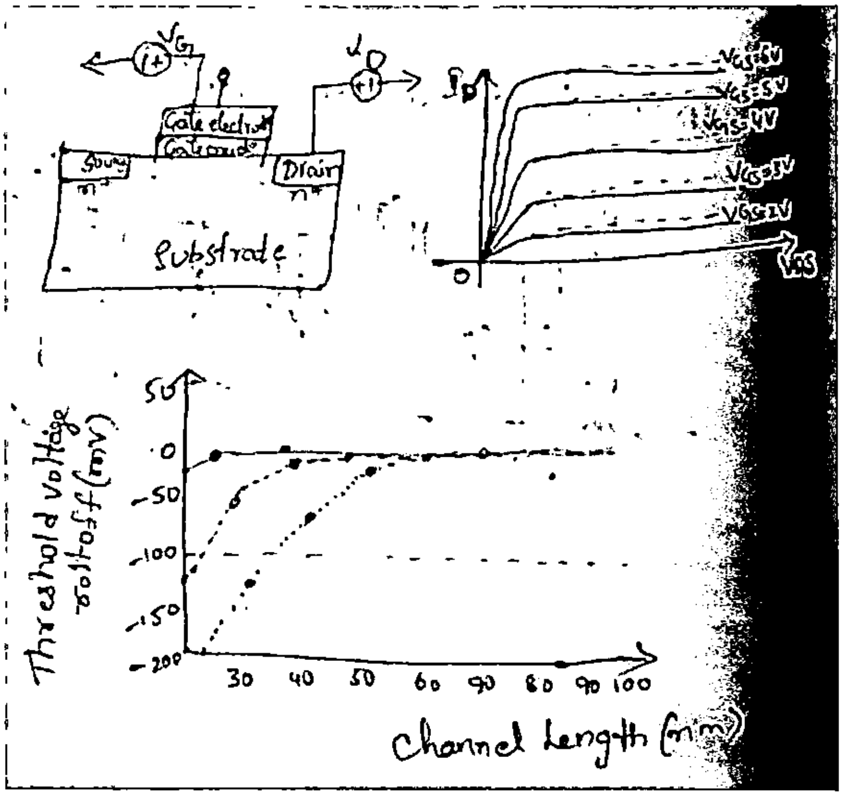
- Increased lattice scattering.
- Reduced drain current.

μ∝T−m\mu \propto T^{-m}μ∝T−m

Where m≈1.5m \approx 1.5m≈1.5

Combined Impact on Device

- Higher temperature → higher leakage.
- Lower mobility → reduced drive current.
- Overall reliability degradation.



6. Temperature effects on MOSFET:

Temperature Effects on MOSFET

Temperature significantly affects MOSFET electrical characteristics and reliability.

1. Mobility Decreases with Temperature

- Carrier mobility reduces due to increased **lattice (phonon) scattering.**
- As temperature rises, atoms vibrate more, increasing collisions.

μ∝T−m(m≈1.5)\mu \propto T^{-m} \quad (m \approx1.5)μ∝T−m(m≈1.5)

Effect:

- Drain current decreases.
- Transconductance (gm) reduces.
- Switching speed reduces.

2. Threshold Voltage (Vth) Decreases Slightly

Threshold voltage reduces with temperature because:

- Fermi potential decreases.
- Intrinsic carrier concentration increases.

dVthdT≈−1 to −3 mV/°C\frac{dV_{th}}{dT} \approx -1 \text{ to } -3 \text{ mV/°C}dTdVth ≈−1 to −3 mV/°C

Effect:

- Device turns ON more easily.
- Contributes to increased leakage.

3. Leakage Current Increases Exponentially

Subthreshold current depends on intrinsic carrier concentration:

ni∝e−Eg/2kTn_i \propto e^{-E_g/2kT}ni∝e−Eg/2kT

As temperature increases:

- nin_ini increases exponentially.
- Subthreshold leakage increases rapidly.

Consequence:

- Higher standby power.
- Thermal runaway risk in dense circuits.

4. Subthreshold Slope Degrades

Subthreshold slope:

S=(ln10)kTq(1+CdCox)S = (ln10)\frac{kT}{q} \left(1 + \frac{C_d}{C_{ox}}\right)S=(ln10)qkT(1+CoxCd)

Since kT/qkT/qkT/q increases with temperature:

S↑ as T↑S \uparrow \text{ as } T \uparrowS↑ as T↑

Effect:

- Poor switching sharpness.
- Higher off-state current.

5. Saturation Current Reduces at High Temperature

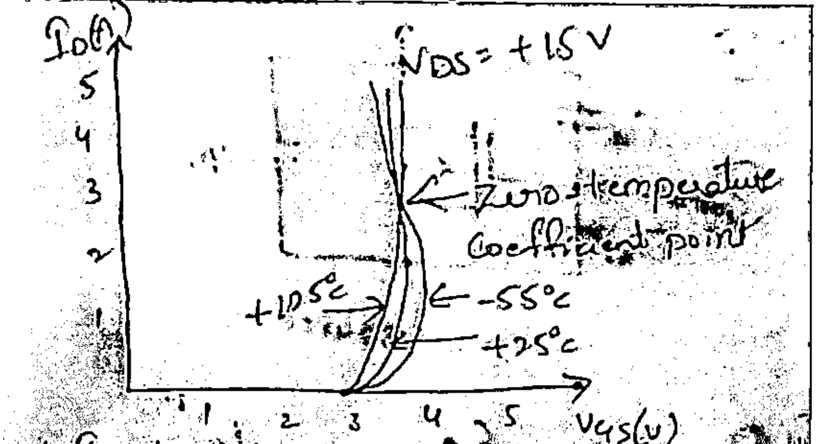
Saturation current:

ID∝μ(VGS−Vth)2I_D \propto \mu (V_{GS} - V_{th})^2ID∝μ(VGS−Vth)2

Although VthV_{th}Vth decreases slightly, mobility reduction dominates.

Result:

- Overall drain current decreases at high temperature.
- Reduced performance in analog and digital circuits.



V-I Character of power MOSFET

7. (a) Meyer capacitance model and small-signal model:

Meyer Capacitance Model and Small-Signal Model

1. Meyer Capacitance Model

The **Meyer model** is a simplified model used in SPICE to represent **MOSFET gate capacitances.**

It divides the total gate capacitance into:

- CgsC_{gs}Cgs (Gate–Source capacitance)
- CgdC_{gd}Cgd (Gate–Drain capacitance)
- CgbC_{gb}Cgb (Gate–Bulk capacitance)

The capacitance values depend on the **region of operation.**

(a) Cutoff Region (VGS < Vth)

- No inversion channel.
- Gate capacitance mainly appears between gate and bulk.

Cgb≈CoxC_{gb} \approx C_{ox}Cgb≈CoxCgs≈0,Cgd≈0C_{gs} \approx 0, \quad C_{gd} \approx 0Cgs≈0,Cgd≈0

(b) Linear (Triode) Region

- Channel formed.
- Gate capacitance shared between source and drain.

Cgs≈23CoxC_{gs} \approx \frac{2}{3} C_{ox}Cgs≈32CoxCgd≈13CoxC_{gd} \approx \frac{1}{3} C_{ox}Cgd≈31CoxCgb≈0C_{gb} \approx 0Cgb≈0

(c) Saturation Region

- Channel pinched off near drain.
- Capacitance mainly toward source.

Cgs≈23CoxC_{gs} \approx \frac{2}{3} C_{ox}Cgs≈32CoxCgd≈0C_{gd} \approx 0Cgd ≈0Cgb≈0C_{gb} \approx 0Cgb≈0

Importance of Meyer Model

- Simple and computationally efficient.
- Used in early SPICE models.
- Does not include charge conservation (limitation).

2. Small-Signal Model of MOSFET

Used for AC and analog analysis.

Small-Signal Parameters

1. **Transconductance (gm)**

gm=∂ID∂VGSg_m = \frac{\partial I_D}{\partial V_{GS}}gm=∂VGS∂ID

Measures gate control over drain current.

2. **Output Conductance (gds)**

gds=∂ID∂VDSg_{ds} = \frac{\partial I_D}{\partial V_{DS}}gds=∂VDS∂ID

Represents channel length modulation.

3. **Capacitances**

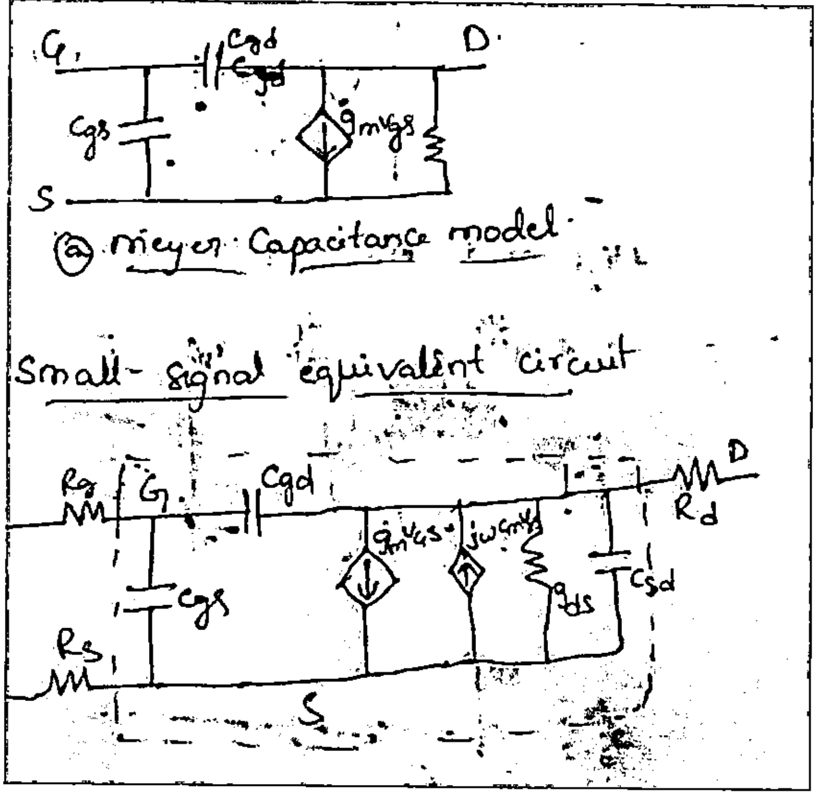
- CgsC_{gs}Cgs
- CgdC_{gd}Cgd (causes Miller effect)
- CdbC_{db}Cdb
- CsbC_{sb}Csb

Complete Small-Signal Model Includes:

- Controlled current source gmvgsg_m v_{gs}gmvgs
- Output resistance ro=1/gdsr_o = 1/g_{ds}ro=1/gds
- Capacitances Cgs,Cgd,Cdb,CsbC_{gs}, C_{gd}, C_{db}, C_{sb}Cgs,Cgd,Cdb,Csb

Applications

- Amplifier gain calculation
- Frequency response analysis
- Stability analysis
- High-frequency modelling



7 (b) Subthreshold slope and leakage:

Subthreshold Slope and Leakage Mechanisms

1. Subthreshold Slope (S)

Definition:

Subthreshold slope (S) indicates how effectively a MOSFET can switch OFF.
It represents the gate voltage required to change drain current by **one decade (10×)** in subthreshold region.
S=(ln10)kTq(1+CdCox)S = (\ln 10)\frac{kT}{q}\left(1 + \frac{C_d}{C_{ox}}\right)S=(ln10)qkT(1+CoxCd)
Where:

- kkk = Boltzmann constant
- TTT = Temperature
- qqq = Electron charge

- CdC_dCd = Depletion capacitance
- CoxC_{ox}Cox = Oxide capacitance

At Room Temperature (300K):

Smin≈60 mV/decadeS_{min} \approx 60 \text{ mV/decade}Smin≈60 mV/decade

This is the **theoretical minimum** for a conventional MOSFET.

Key Observations:

- Higher CdC_dCd → Larger S → Poor switching
- Higher CoxC_{ox}Cox → Smaller S → Better switching
- Increasing temperature → S increases

Lower subthreshold slope → sharper switching → lower leakage.

2. Leakage Mechanisms in MOSFET

As devices scale, leakage current becomes significant.

(a) Subthreshold Conduction

- Occurs when VGS<VthV_{GS} < V_{th}VGS<Vth.
- Current flows due to diffusion of carriers.
- Exponential dependence:

Isub∝eVGSnVTI_{sub} \propto e^{\frac{V_{GS}}{nV_T}}Isub∝enVTVGS

Major contributor to standby power.

(b) Gate Oxide Tunneling

- Caused by ultra-thin oxide layers.
- Electrons tunnel through oxide.
- Includes:
    - Direct tunneling
    - Fowler–Nordheim tunneling

Increases drastically with oxide scaling.

(c) Junction Leakage

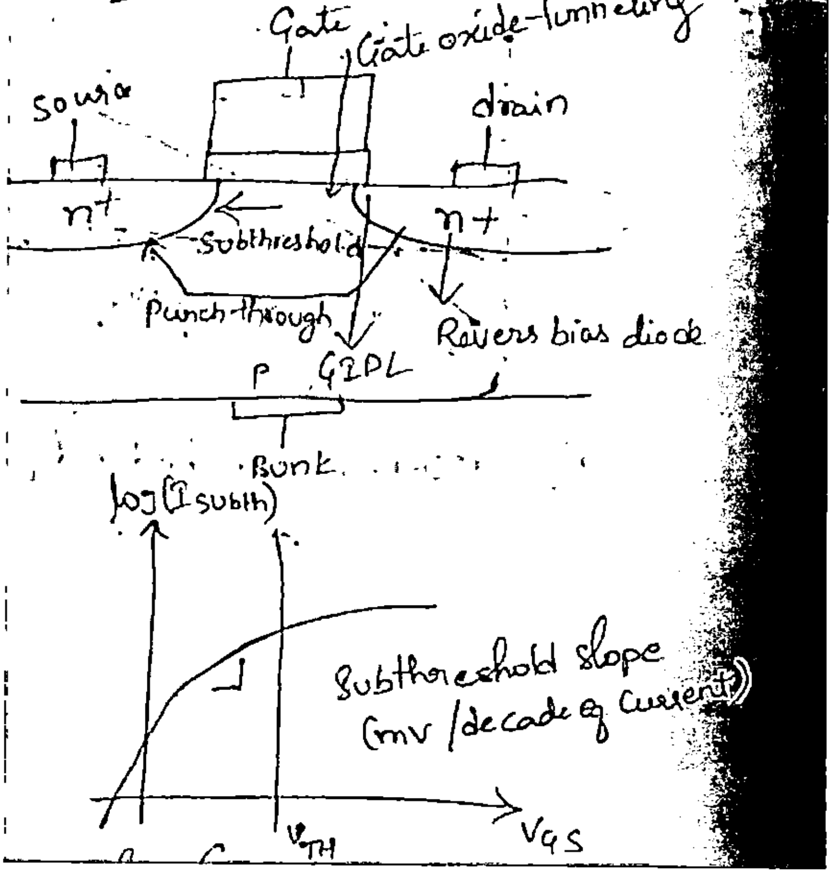
- Reverse-biased source-body and drain-body junctions.
- Due to:
    - Minority carrier diffusion
    - Generation-recombination
    - Band-to-band tunneling

Increases with temperature.

(d) GIDL (Gate Induced Drain Leakage)

- Occurs at high drain voltage and low gate voltage.
- Strong electric field near drain causes band-to-band tunneling.
- Prominent in short-channel devices.

Fig:- Subthreshold Slope & leakage mech



8. (a) Hot-carrier and interface trap generation:

Hot-carrier effects (HCE) and the resulting interface trap generation are among the most critical reliability challenges in modern, scaled-down metal-oxide-semiconductor field-effect transistors (MOSFETs)

. As gate lengths shrink, high lateral electric fields near the drain accelerate electrons to high kinetic energies ("hot carriers"), enabling them to cross the Si-SiO$_2$ barrier or create defects, causing long-term device degradation.

1. Hot-Carrier Effects (HCE)

Mechanism:

- **Carrier Acceleration:** In short-channel MOSFETs, the high lateral electric field near the drain accelerates electrons to high velocities.
- **Injection:** These "hot" electrons gain enough energy to surmount the Si-SiO$_2$ potential barrier ($\sim$3.1 eV for electrons, $\sim$4.6 eV for holes) and become trapped in the gate oxide.
- **Impact Ionization:** Hot carriers can strike the silicon lattice, causing impact ionization (creating electron-hole pairs). This generates a large substrate current and, in n-MOSFETs, injects hot electrons into the oxide.
- **Worst-Case Condition:** For n-MOSFETs, maximum hot-carrier degradation typically occurs at

, where the substrate current is maximized.

Impact on Performance:

- **Shift:** Trapped electrons in the oxide create a negative charge, causing a positive shift in threshold
- **Reduced Mobility &:** The generated traps act as scattering centers, decreasing carrier mobility

Lowered Drain: The combined effects lead to decreased drain current, resulting in slower circuit switching speeds.

2. Interface Trap Generation

Mechanism:

- **Si-H Bond Breaking:** Hot carriers, particularly those moving along the channel, dissociate Si-H bonds at the Si-SiO_2 interface.
- **Trap Creation:** The dissociation creates dangling silicon bonds that act as interface
- **Reaction-Diffusion (R-D) Model:** Under electrical stress, these traps generate hydrogen atoms, which diffuse into the oxide.
- **Saturation Behavior:** While interface trap generation initially follows a power law with, it shows saturation behavior after longer stress times.

3. Evaluation of HCE and Interface Traps

- **Dominant Degradation Source:** While both oxide charging and interface traps degrade performance, studies indicate that interface trap generation is the dominant degradation mechanism in many stress conditions, particularly in n-MOSFETs.
- **Long-Term Reliability:** HCE is a cumulative, non-reversible aging process. It accounts for 40-80% of all transistor aging after 10 years of operation.
- **Scaling Limitations:** As gate oxide thicknesses shrink in nanoscale devices, hot-carrier problems persist because, while lower supply voltages reduce maximum energy, increased channel fields still produce sufficient "hot" electrons.
- **Mitigation Techniques:**
  - **Lightly Doped Drains (LDD):** Creating a more gradual voltage drop near the drain reduces the electric field intensity.

Advanced Structures: FinFETs and Gate-All-Around (GAA) FETs provide better electrostatic control but may suffer from severe self-heating, which can exacerbate HCI degradation.

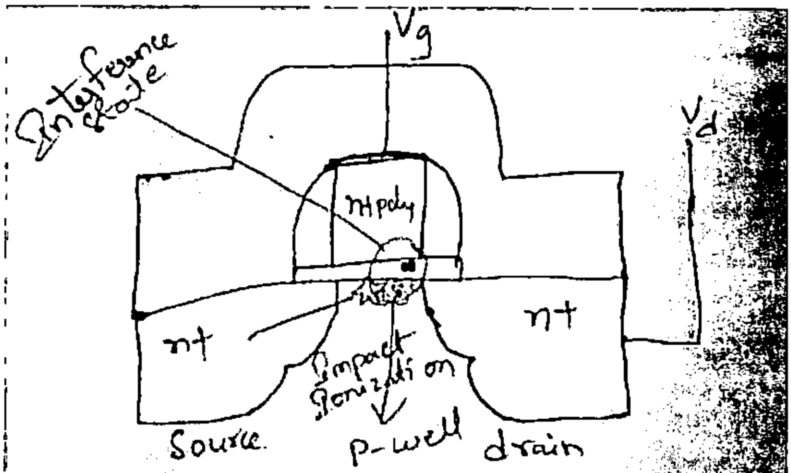


fig:- Hot - carrier

8 (b) SPICE parameter extraction and calibration:

SPICE parameter extraction and model calibration are critical processes in semiconductor device modeling, bridging the gap between theoretical compact models (like BSIM, PSP) and the real-world performance of manufactured devices. These techniques are used to ensure that circuit simulations (in LTspice, HSPICE, etc.) accurately predict the behavior of electronic circuits.

1. SPICE Parameter Extraction

Parameter extraction is the process of obtaining the numerical values for the parameters in a SPICE model card from measured electrical data (DC and AC).

- **Data Collection (Measurement):**
    - **DC Measurements:** Using a semiconductor parameter analyzer to generate current-voltage (I-V) characteristics, such as drain current (Id) versus gate-source voltage (Vgs) and Id versus drain-source voltage (Vds) for various transistor geometries (W/L).
    - **AC Measurements:** Using capacitance-voltage (C-V) meters to measure capacitances and high-frequency analyzers for small-signal parameters.
- **Extraction Techniques:**
    - **Direct Extraction:** Parameters are extracted directly from measured data using simplified analytical equations. For example, the threshold voltage (Vt) is determined from the I-V characteristics using linear extrapolation of the transfer curve (Id vs. Vgs) in the linear region.
    - **Optimization-Based Extraction:** For complex, high-dimensional models (e.g., BSIM4), numerical optimization algorithms (like Levenberg-Marquardt) are used to minimize the error between simulated and measured data across multiple measurement sets.
    - **Numerical Differentiation:** Used to calculate parameters like transconductance (gm=d*Id/d*Vgs).

- **Key Parameters Extracted:**
    - **MOSFETs:** Threshold voltage (Vto) transconductance coefficient (KP
    - **Diodes:** Saturation current (Is), ideality factor (n), and series resistance (Rs).

2. Model Calibration Techniques

Model calibration ensures that the extracted parameters, which might be "local" (specific to one device), are adjusted to represent a "global" model that accounts for manufacturing variations across different geometries and temperatures.

- **Geometry Dependence Modeling:** The extraction of parameters is repeated for devices with different channel lengths (L) and widths (W) to model the scaling behavior, allowing the model to accurately predict performance for various transistor sizes.
- **Optimization & Fitting:**
    - **Global Optimization:** A comprehensive optimization is performed to minimize the error between simulations and measurements across all device geometries and bias conditions simultaneously.
- **De-embedding Procedures:** To ensure the model reflects the actual device, parasitic effects from test pads and interconnects (measured using "open" and "short" structures) are removed from the raw measured data before parameter extraction.
- **Validation:** The calibrated model is validated by comparing simulated results with experimental data for circuits like inverters or ring oscillators.

3. Workflow for Model Development

1. **Fabrication and Measurement:** Fabricate devices and measure I-V/C-V data.
2. **Initial Parameter Extraction:** Perform direct extraction of key parameters.
3. **Optimization:** Use iterative algorithms to refine parameters to match measured data.
4. **Verification:** Compare the final SPICE model simulation with the measured, real-device performance.
5. **Model Card Generation:** Create the finalized SPICE model file for circuit simulation.

Techniques such as using genetic algorithms or automated machine-learning approaches are increasingly used for faster, more accurate, and global parameter optimization.

9. (a) Gate oxide reliability:

Gate oxide reliability is a critical concern in MOS-based devices (like MOSFETs), especially as oxide thickness scales down into the nanometer range. The gate oxide (typically SiO_2 or high-k dielectric) must maintain strong insulation while withstanding high electric fields over long operating times.

Below is a structured analysis of key reliability concerns.

1. Oxide Breakdown

(a) Time-Dependent Dielectric Breakdown (TDDB)

- Caused by prolonged high electric field across the oxide.
- Defects accumulate over time due to charge trapping.
- Eventually forms a conductive path → catastrophic failure.

Mechanism:

1. High electric field generates traps.
2. Traps accumulate and percolate.
3. Sudden breakdown occurs.

Impact:

- Permanent device failure.

- Reduced lifetime of ICs.

(b) Hard vs Soft Breakdown

- **Soft Breakdown (SBD):** Partial leakage increase; device may still function.
- **Hard Breakdown (HBD):** Complete dielectric failure; short between gate and channel.

As oxide thickness decreases, soft breakdown becomes more common.

2. High Electric Field Effects

(a) Fowler–Nordheim Tunneling

In very thin oxides:

- Electrons tunnel through the oxide under high electric field.
- Causes stress-induced damage and charge trapping.

Leads to:

- Increased gate leakage.
- Long-term reliability degradation.

(b) Direct Tunneling

When oxide thickness < ~3 nm:

- Electrons tunnel even at low voltages.
- Results in high standby power and oxide wear-out.

3. Charge Trapping

Charges may get trapped:

- In the oxide bulk
- At the Si–SiO_2 interface

Effects:

- Threshold voltage (Vt) shift
- Mobility degradation
- Increased subthreshold slope
- Device parameter drift over time

This is especially critical in:

- Flash memory
- High-field analog circuits

4. Hot Carrier Injection (HCI)

- High-energy carriers near drain gain enough energy to enter the oxide.
- Causes:
    - Interface state generation
    - Oxide trapped charge
    - Vt shift

Common in:

- Short-channel MOSFETs
- High-speed digital circuits

5. Bias Temperature Instability (BTI)

(a) Negative BTI (NBTI)

- Affects PMOS under negative gate bias.
- Causes interface trap formation.
- Results in threshold voltage increase.

(b) Positive BTI (PBTI)

- Affects NMOS (especially with high-k dielectrics).
- Causes Vt shift and mobility degradation.

Temperature accelerates degradation.

6. Radiation Effects

Ionizing radiation:

- Generates electron-hole pairs in oxide.
- Holes get trapped.
- Causes threshold shift and leakage increase.

Important in:

- Space electronics
- Nuclear environments

7. Scaling Challenges

As technology scales:

- Oxide thickness ↓
- Electric field ↑
- Leakage current ↑
- Reliability margin ↓

High-k dielectrics (e.g., HfO_2) are used to:

- Maintain capacitance
- Increase physical thickness
- Reduce tunneling

However, high-k materials introduce:

- More trap sites
- BTI sensitivity

8. Reliability Modeling

Common reliability models:

- E-model (field-driven)
- 1/E model
- Power law model

Used to predict:

- Time to breakdown (TTBD)
- Lifetime under operating conditions

Accelerated stress testing is used to extrapolate lifetime.

9 (b) MOSFET simulation using SPICE:

SPICE (Simulation Program with Integrated Circuit Emphasis) is a circuit simulation tool used to analyze MOSFET characteristics such as output characteristics (ID–VDS), transfer characteristics (ID–VGS), threshold voltage, and transconductance. It helps in predicting device performance before fabrication.

1. MOSFET Representation in SPICE

The general syntax for MOSFET in SPICE is:

Mname Drain Gate Source Bulk ModelName L= W=

Example:

```
M1 D G S B NMOS L=1u W=10u
```

Where:
D = Drain
G = Gate
S = Source
B = Bulk
L = Channel length
W = Channel width

2. MOSFET Model Definition

The MOSFET parameters are defined using the .MODEL statement:

```
.MODEL NMOS NMOS (VTO=0.7 KP=200u LAMBDA=0.02 GAMMA=0.4 PHI=0.7)
```

Important Parameters:

- VTO → Threshold voltage
- KP → Transconductance parameter (μnCox)
- LAMBDA → Channel length modulation parameter
- GAMMA → Body effect coefficient
- PHI → Surface potential

3. Simulation of Output Characteristics (ID vs VDS)

Aim: To obtain drain current variation with drain voltage.

SPICE Program:

```
* NMOS Output Characteristics

VDS  D0  0
VGS  G0  2
VS   S  0  0
VB   B  0  0
M1   D  GS  BNMOS  L=1u  W=10u
.MODEL NMOS NMOS (VTO=0.7 KP=200u LAMBDA=0.02)
.DC VDS 0 5 0.1
.PRINT DC I(VDS)
.END
```

Explanation:

- VGS is kept constant at 2 V.
- VDS is swept from 0 to 5 V using .DC command.
- Drain current is measured.

4. Regions of Operation Observed

1. **Cutoff Region:**
   If VGS < VTO → ID ≈ 0
2. **Linear (Triode) Region:**
   If VDS < (VGS − VTO)
3. **Saturation Region:**
   If VDS ≥ (VGS − VTO)

Drain current in saturation region:

ID = (1/2) KP (W/L) (VGS − VTO)² (1 + λVDS)

5. Transfer Characteristics (ID vs VGS)
To obtain threshold voltage:

```
VDS  D0  5
VGS  G  0  0

.DC VGS 0 5 0.1
```

Here VDS is constant and VGS is swept from 0 to 5 V.

10. Explain and analyze mobility and threshold voltage extraction methods.

Introduction

Mobility (μ) and Threshold Voltage (VT) are important MOSFET parameters.

- **Threshold Voltage (VT)** is the minimum gate voltage required to form a conducting channel.
- **Mobility (μ)** determines how fast charge carriers move in the channel and affects drain current.

Accurate extraction of these parameters is necessary for device modeling and circuit design.

Part A: Threshold Voltage (VT) Extraction Methods

1. Linear Extrapolation Method

In the linear region (small VDS):

$$I_D = \mu C_{ox} \frac{W}{L} [(V_{GS} - V_T)V_{DS}]$$

Procedure:

1. Measure ID vs VGS at small VDS.
2. Plot ID versus VGS.
3. Extend the linear portion of the curve to ID = 0.
4. The intercept on VGS axis gives VT.

Merits: Simple and widely used.
Limitation: Affected by mobility degradation and series resistance.

2. √ID Method (Saturation Region Method)

In saturation:

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

Taking square root:

$$\sqrt{I_D} \propto (V_{GS} - V_T)$$

Advantage: More accurate for long-channel devices.

3. Transconductance (gm) Method

$$g_m = \frac{dI_D}{dV_{GS}}$$

Procedure:

1. Measure ID vs VGS.

2. Calculate gm.
3. Draw tangent at maximum gm.
4. Intercept on VGS axis gives VT.

Advantage: Provides better accuracy.

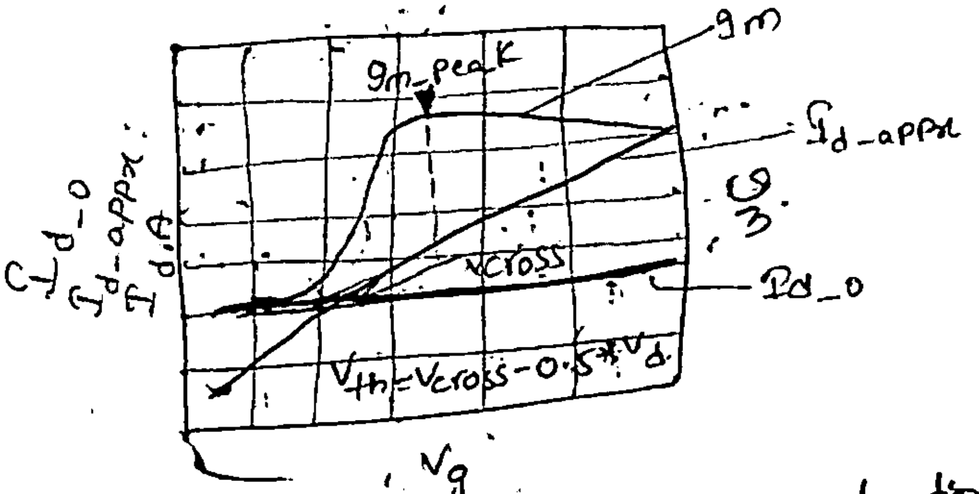


fig:- MOSFET Threshold voltage extraction

Part B: Mobility (µ) Extraction Methods

Mobility is extracted from drain current equations.

1. Mobility from Linear Region

In linear region:

$$I_D = \mu C_{ox} \frac{W}{L} [(V_{GS} - V_T)V_{DS}]$$

Rearranging:

$$\mu = \frac{L}{W C_{ox} V_{DS}} \cdot \frac{I_D}{(V_{GS} - V_T)}$$

Procedure:

1. Measure ID at known VGS and VDS.
2. Use extracted VT.
3. Substitute values to calculate µ.

2. Mobility Using Transconductance (gm Method)

In linear region:

$$g_m = \mu C_{ox} \frac{W}{L} V_{DS}$$

Therefore,

$$\mu = \frac{g_m L}{W C_{ox} V_{DS}}$$

Procedure:

1. Determine gm from slope of ID vs VGS curve.
2. Substitute values to calculate μ.

Advantage: More accurate and less error-prone.

10. Mobility and threshold extraction methods:

Mobility (μ) and Threshold Voltage (VT) are important MOSFET parameters.

- **Threshold Voltage (VT)** is the minimum gate voltage required to form a conducting channel.
- **Mobility (μ)** determines how fast charge carriers move in the channel and affects drain current.

Accurate extraction of these parameters is necessary for device modeling and circuit design.

Part A: Threshold Voltage (VT) Extraction Methods

1. Linear Extrapolation Method

In the linear region (small VDS):

$$I_D = \mu C_{ox} \frac{W}{L} [(V_{GS} - V_T) V_{DS}]$$

Procedure:

5. Measure ID vs VGS at small VDS.
6. Plot ID versus VGS.
7. Extend the linear portion of the curve to ID = 0.
8. The intercept on VGS axis gives VT.

Merits: Simple and widely used.

Limitation: Affected by mobility degradation and series resistance.

2. √ID Method (Saturation Region Method)

In saturation:

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

Taking square root:

$$\sqrt{I_D} \propto (V_{GS} - V_T)$$

Procedure:

1. Plot √ID vs VGS.
2. Extend straight-line portion to √ID = 0.
3. Intercept on VGS axis gives VT.

Advantage: More accurate for long-channel devices.

3. Transconductance (gm) Method

$$g_m = \frac{dI_D}{dV_{GS}}$$

Procedure:

5. Measure ID vs VGS.
6. Calculate gm.
7. Draw tangent at maximum gm.
8. Intercept on VGS axis gives VT.

Advantage: Provides better accuracy.

Part B: Mobility (μ) Extraction Methods

Mobility is extracted from drain current equations.

1. Mobility from Linear Region

In linear region:

$$I_D = \mu C_{ox} \frac{W}{L} [(V_{GS} - V_T)V_{DS}]$$

Rearranging:

$$\mu = \frac{L}{W C_{ox} V_{DS}} \cdot \frac{I_D}{(V_{GS} - V_T)}$$

Procedure:

4. Measure ID at known VGS and VDS.
5. Use extracted VT.
6. Substitute values to calculate μ.

2. Mobility Using Transconductance (gm Method)

In linear region:

$$g_m = \mu C_{ox} \frac{W}{L} V_{DS}$$

Therefore,

$$\mu = \frac{g_m L}{W C_{ox} V_{DS}}$$

Procedure:

3. Determine gm from slope of ID vs VGS curve.
4. Substitute values to calculate μ.

Advantage: More accurate and less error-prone.

11(a) Worst-case corner modeling:

In VLSI design, device parameters vary due to **process, voltage, and temperature (PVT) variations.**

Worst-case corner modeling is used to ensure that circuits function correctly under extreme operating conditions.

A **corner** represents a set of extreme parameter values used during simulation.

1. Need for Worst-Case Corner Modeling

Due to fabrication variations:

- Threshold voltage (VT) varies
- Mobility (μ) varies

- Oxide thickness varies
- Channel length varies
- Supply voltage fluctuates
- Temperature changes

These variations affect:

- Speed
- Power consumption
- Leakage
- Noise margins

Therefore, worst-case modeling ensures reliable circuit performance.

2. Types of Process Corners

Process corners represent variations in NMOS and PMOS performance.

Common Corners:

1. **TT (Typical-Typical)**
   - Both NMOS and PMOS have nominal parameters.
2. **FF (Fast-Fast)**
   - Both NMOS and PMOS are faster than nominal.
   - Lower VT, higher mobility.
   - Results in higher speed and higher leakage.
3. **SS (Slow-Slow)**
   - Both NMOS and PMOS are slower.
   - Higher VT, lower mobility.
   - Results in lower speed and reduced leakage.
4. **FS (Fast-Slow)**
   - NMOS fast, PMOS slow.
5. **SF (Slow-Fast)**
   - NMOS slow, PMOS fast.

These corners are provided in technology libraries for simulation.

3. Voltage and Temperature Corners

(A) Voltage Corners

- VDD_max → Higher speed, higher power
- VDD_min → Slower operation, possible timing failure

(B) Temperature Corners

- High temperature → Reduced mobility, slower circuit
- Low temperature → Increased speed, higher leakage in some cases

11 (b) Yield estimation techniques:

Introduction

Yield in VLSI design is defined as the percentage of functional chips obtained from the total number of fabricated chips on a wafer.

$$\text{Yield} = \frac{\text{Number of good chips}}{\text{Total chips fabricated}} \times 100$$

Yield estimation is important because it directly affects **manufacturing cost, profitability, and reliability** of ICs.

1. Types of Yield

1. **Wafer Yield** – Fraction of non-defective dies on a wafer.
2. **Functional Yield** – Fraction of dies meeting performance specifications.
3. **Parametric Yield** – Fraction of dies within acceptable electrical limits.

2. Yield Estimation Techniques

1. Poisson Yield Model

Assumes defects occur randomly over the wafer.

$$Y = e^{-AD}$$

Where:
A = Chip area
D = Defect density (defects per unit area)

Analysis:

- Larger chip area → Lower yield
- Higher defect density → Lower yield
- Simple and widely used model

Limitation: Assumes defects are uniformly distributed.

2. Murphy's Yield Model

Considers non-uniform defect distribution.

$$Y = \left(\frac{1 - e^{-AD}}{AD}\right)$$

Analysis:

- Gives higher yield than Poisson model
- More realistic for practical manufacturing
- Accounts for partial defect clustering

3. Negative Binomial Model

Used when defects are clustered.

$$Y = \left(1+\frac{AD}{\alpha}\right)^{-\alpha}$$

Where:
α = Clustering parameter

Analysis:

- More accurate for modern VLSI processes
- Accounts for defect clustering
- Widely used in advanced technology nodes

4. Monte Carlo Simulation

Statistical method used to estimate yield.

Procedure:

1. Randomly vary process parameters (VT, L, W, oxide thickness).
2. Simulate circuit multiple times.
3. Calculate percentage of circuits meeting specifications.

5. Corner-Based Yield Estimation

- Simulate circuits at worst-case PVT corners.
- Check if design meets specifications at all corners.

3. Factors Affecting Yield

- Chip area
- Defect density
- Process variations
- Lithography limitations
- Contamination
- Design complexity

Larger die size reduces yield significantly.