Code No.: R25EC57111PE	R25	H.T.No.			8	R						

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–I–Semester End Examinations (Regular) - February- 2026
DEVICE MODELING
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a)	Define scaling and list its benefits.	[2M]
b)	Define narrow-width effect.	[2M]
c)	Outline What is mobility degradation?	[2M]
d)	Define hot-carrier degradation.	[2M]
e)	Demonstrate any two threshold voltage extraction methods.	[2M]

PART-B **(50 Marks)**

2.	Explain the impact of scaling effects on device performance in modern VLSI design.	[10M]
	OR	
3.a)	Illustrate parasitic capacitances in MOSFET.	[5M]
b)	Analyze modern multi-gate MOSFET structures.	[5M]
4.a)	Derive flat-band voltage and threshold voltage expressions.	[5M]
b)	Interpret and analyze high-frequency and low-frequency C–V characteristics.	[5M]
	OR	
5.a)	Examine DIBL and channel length modulation.	[5M]
b)	Explain the short channel effects and its influence on device characteristics like threshold voltage and temperature.	[5M]
6.	Explain and assess temperature effects on MOSFET current characteristics.	[10M]
	OR	
7.a)	Construct the Meyer capacitance model and small-signal equivalent circuit.	[5M]
b)	Analyze sub-threshold slope and leakage mechanisms.	[5M]
8.a)	Explain and evaluate hot-carrier effects and interface trap generation.	([5M]
b)	Describe SPICE parameter extraction and model calibration techniques.	[5M]
	OR	
9.a)	Analyze gate oxide reliability concerns.	[5M]
b)	Demonstrate MOSFET simulation using SPICE parameters.	[5M]
10.	Explain and analyze mobility and threshold voltage extraction methods.	[10M]
	OR	
11.a)	Discuss worst-case corner modeling approaches.	[5M]
b)	Assess yield estimation techniques in VLSI design.	[5M]

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