Code No.: R22EC57202PC | R22 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Supply) – February 2026
LOW POWER SYSTEM DESIGN
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a)	Illustrate the main sources of power dissipation in CMOS circuits.	[1M]
b)	How does supply voltage (V_{dd}) affect power consumption?	[1M]
c)	Describe energy recovery in low-power circuit design.	[1M]
d)	Discuss briefly about low power clock distribution.	[1M]
e)	List two power minimization techniques in digital circuits.	[1M]
f)	What is operand isolation in low-power circuit design?	[1M]
g)	Give the significance of low power memory design.	[1M]
h)	How does power dissipation occur in DRAM circuits?	[1M]
i)	What are the recent trends in low-power microprocessor architectures?	[1M]
j)	Define dynamic voltage and frequency scaling,	[1M]

PART-B **(50 Marks)**

2.	Explain the challenges and benefits of technology scaling in low-power VLSI design.	[10M]
	OR	
3.	Discuss emerging low-power approaches and their advantages in modern IC design.	[10M]
4.	Discuss the impact of latches and flip-flops in power consumption	[10M]
	OR	
5.	Explain the importance of single-driver clock distribution and clock gating in low-power design.	[10M]
6.a)	Illustrate the DTCMOS techniques to minimize the power in VLSI circuits.	[6M]
b)	Write the advantages and disadvantages of DTCMOS technique.	[4M]
	OR	
7.	Draw and explain the logic circuit of the CMOS full adder.	[10M]
8.	Describe various sources of power dissipation in memory subsystems.	[10M]
	OR	
9.	Discuss different circuit-level and architectural techniques used for low-power DRAM design.	[10M]
10.	Discuss the architectural trade-offs for power-efficient microprocessor design.	[10M]
	OR	
11.	Describe how does dynamic voltage and frequency scaling (DVFS) help in reducing power.	[10M]

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