Code No: 54010 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year II Semester Examinations, May - 2015
SWITCHING THEORY AND LOGIC DESIGN
(Common to EEE, ECE, BME, ETM)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Explain the procedure for converting Gray code to Binary code with an example.
b) Solve for X
i) $(F3A7C2)_{16} = (X)_{10}$
ii) $(2AC5)_{16} = (10949)_X$
iii) $(0.93)_{10} = (X)_8$
iv) $(4057.06)_8 = (X)_{10}$ [7+8]

2.a) Write the Dual of
i) (A+BC'+AB)
ii) (AB+B'C+CD)
b) Prove the following identity
XY + X'Y' +YZ = XY +X'Y' +X'Z. [8+7]

3. Use tabular procedure to simplify the given expression
f(v,w,x,y,z) =∑m(0,4,12,16,19,24,27,28,29,31) in SOP form and draw the circuit using only NAND gates. [15]

4.a) Design a logic circuit to encode a 2^n input bits to n bit output.
b) Design a 4 bit Parallel adder using full adders. [8+7]

5. Design a sequential logic circuit of a 4 bit counter to start counting from 0000 to 1000 and this process should go on. Draw the ASM chart and design the Data processing unit and the control unit. [15]

6.a) Draw the block diagram of a ROM. Define address and word. Relate the number of output lines with number of bits in a word. How an output word can be selected?
b) For a 64×8 ROM, determine the number of words it contains and the size of each word. How many output lines are there for the ROM? [7+8]

7.a) Give a detailed comparison between combinational logic circuits and sequential logic circuits.
b) Explain the operation of JK flip flop with the help of input output waveforms. [8+7]