Code No: 113BU **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, May/June - 2015
SWITCHING THEORY AND LOGIC DESIGN
(Common to ECE, EIE)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks.

PART- A

(25 Marks)

1.a) Find the complement of (AB'+C)D'+E. [2M]
b) What are single error detecting codes and how error detection is accomplished? [3M]
c) What are static hazards? [2M]
d) Explain the six variable Karnaugh map. [3M]
e) Define sequential circuit and give example. [2M]
f) Explain about clocked T flip-flop. [3M]
g) What is the difference between synchronous and asynchronous Sequential circuits? [2M]
h) A 3-bit binary ripple counter uses T -flip-flops that trigger on the negative edge of the clock. What will be the count if complement outputs of the flip-flop are connected to the clock? Draw the timing waveform. [3M]
i) What is the difference between flow chart and ASM chart? [2M]
j) What are the capabilities of finite state machine? [3M]

PART-B

(50 Marks)

2.a) Find the 16's complement of AF3B.
b) Formulate a weighted binary code for the decimal digits using weights 6,3,1,1.
c) Implement F=(AB'+A'B)(C+D') using NAND gates. [2+4+4]

OR

3.a) Convert decimal 9126 to both BCD and ASCII codes.
b) Show that a positive logic NAND gate is a negative logic NOR gate and vice versa.
c) Express the complement of $F(A,B,C,D)=\sum(0,2,6,11,13,14)$ in sum of min terms. [2+4+4]

4.a) Use the tabulation procedure to generate the set of prime implicants and to obtain all minimal expressions for the function:
$F(w,x,y,z)=\sum(0,1,4,5,6,7,9,11,15)+\sum\varphi(10,14)$
b) Implement the function $F(A,B,C,D)=\sum(0,1,3,4,6,8,15)$ using required capacity decoder and logic gates. [5+5]

OR

5.a) Design a BCD adder.
b) Find all the prime implicants for the Boolean function:
$F(w,x,y,z)=\sum(1,3,4,5,10,11,12,13,14,15)$ and find which are essential. [5+5]

6.a) With a neat diagram explain about D-Type positive edge triggered flip-flop.

b) Design a T flip-flop using JK flip-flop. Use k-maps for the design. [5+5]

OR

7.a) What is the difference between edge triggering and level triggering? Explain about Edge triggered JK flip-flop with a neat diagram.

b) Design a JK flip-flop using SR flip-flop. Use k-maps for the design. [5+5]

8.a) Design a sequential circuit with two D flip-flops A and B, and one input x. When x=0, the state of the circuit remains same. When x=1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats.

b) List the basic types of shift registers in terms of data movement. [8+2]

OR

9.a) Design a divide by 6 ripple counter using T flip-flops.

b) Design a counter using JK flip-flops with the repeated binary sequence 0,1,2,3,4,5,6. [5+5]

10.a) Explain the state minimization using merger graph and merger table.

b) Explain the multiplexer method of implementing ASM charts. [5+5]

OR

11.a) Determine the minimal state table equivalent to the state table given:

PS	NS,Z	
	x=0	x=1
A	A,1	E,0
B	A,0	E,0
C	B,0	F,0
D	B,0	F,0
E	C,0	F,1
F	C,0	F,1
G	D,0	H,1
H	D,0	H,1

b) Draw the ASM chart and state table for a 2-bit counter having one enable line E such counting is enabled when E=1 and counting is disabled when E=0. [5+5]

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