R13

LINEAR AND DIGITAL IC APPLICATIONS
(Common to BME, ECE, ETM)

Time: 3 hours   **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A
(25 Marks)

1.a)   Show the standard representation of IC voltage regulator.   [2]
  b)   Explain the precautions that can be taken to minimize the effect of noise on an OP-AMP circuit.   [3]
  c)   Define stable and quasi stable state.   [2]
  d)   Draw the circuit diagram of Second order high pass filter and give its transfer function.   [3]
  e)   List out different types of A/D converters.   [2]
  f)   What do you mean by quantization error in an A/D converter?   [3]
  g)   Give the working principle of analog multiplexer.   [2]
  h)   How to interface the TTL logic gates to the CMOS logic?   [3]
  i)   What is meant by state diagram?   [2]
  j)   Write the specifications of counter IC's.   [3]

PART - B
(50 Marks)

2.   Design a differentiator circuit that will differentiate input signal with f_{max} = 100Hz.
                                                                                    [10]

OR

3.a)   What are the differences between the inverting and non inverting terminals? What do you mean by the term "virtual ground"?
  b)   Explain the method of boosting the current of a three terminal voltage regulator.   [5+5]

4.   Design and explain the operation of All Pass Filter with its characteristics.   [10]

OR

5.a)   Draw the circuit of Schmitt trigger using 555 timer and explain its operation.
  b)   Draw the circuit of a PLL AM detector and explain its operation.   [5+5]

6.   Draw the schematic block diagram of Dual-slope A/D converter and explain its operation. Derive expression for its output voltage V_o.   [10]

OR

7.a)   What is the conversion time of a 10 bit successive approximation ADC if its input clock is 5 MHz?
  b)   List the specifications of DAC.   [5+5]

8.a) Design a 5 to 32 line decoder using 3 to 8 line decoder, active low outputs with 2 active low and one active high enable.

b) What do you mean by Carry propagation delay? Design a 4-bit Carry look ahead generation circuit? [5+5]

OR

9. Draw and explain the block diagram of n-bit parallel binary adder/subtractor. [10]

10.a) Explain operation of DRAM cell array.

b) Design and implement FIFO shift register using IC's. [5+5]

OR

11.a) Design and implement 4-bit synchronous down counter using IC.

b) Explain the internal structure of ROM. [5+5]

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