Code No: R05221901 **R05** **Set No. 2**

II B.Tech II Semester Examinations,April/May 2012
COMPUTER ORGANISATION
Common to Instrumentation And Control Engineering, Electronics And Computer Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Why do we need subroutine register in a control unit? Explain.
   (b) Explain nanoinstructions and nanometry. Why do we need them? [8+8]
2. (a) What is pipeline? Give the detailed picture of pipeline.
   (b) Explain pipeline for floating point addition and subtraction. [8+8]
3. Explain the following:
   (a) Peripheral Component Interconnect Bus (PCI)
   (b) Universal Serial Bus (USB) [8+8]
4. Explain the working of the following:
   (a) Page table
   (b) TLB
   (c) Memory Management Unit [5+5+6]
5. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those.
   (b) Explain time-shared common bus Organization.
   (c) Explain system bus structure for multiprocessors [6+5+5]
6. (a) Explain Booth's algorithm with its theoretical basis.
   (b) Represent two n-bit unsigned numbers multiplications with a series of n/2-bit multiplications. [8+8]
7. (a) Find out what are the actual values of the following IEEE 754 single precision number.
      i. Sign=0, exponent=all 1s and fraction field is not 0.
      ii. Sign=0, exponent=all 0s and fraction field is 0.
      iii. Sign=1, exponent=all 1s and fraction field is 0.
      iv. Sign=0, exponent=1000 0001, fraction=1100 0000 0000 0000 0000 000

      [1+1+1+3]
   (b) Why is bus arbitration required. Discuss about any two bus arbitration methods. [10]

8. Explain about instruction, fetch, and decode cycles for a memory reference instruction. Draw a flow chart also to explain the same. Indicate clearly where and which processor registers comes into picture. Now let us assume while a instruction is in the middle of its decode cycle a interrupt is arrived. What is going to happen? Is the instruction completed or not. If we want to stop there itself and handle the interrupt what are the difficulties? [16]

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Code No: R05221901 **R05** **Set No. 4**

II B.Tech II Semester Examinations,April/May 2012
COMPUTER ORGANISATION
Common to Instrumentation And Control Engineering, Electronics And Computer Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Why do we need subroutine register in a control unit? Explain.
   (b) Explain nanoinstructions and nanometry. Why do we need them? [8+8]

2. (a) Find out what are the actual values of the following IEEE 754 single precision number.
      i. Sign=0, exponent=all 1s and fraction field is not 0.
      ii. Sign=0, exponent=all 0s and fraction field is 0.
      iii. Sign=1, exponent=all 1s and fraction field is 0.
      iv. Sign=0, exponent=1000 0001, fraction=1100 0000 0000 0000 0000 000

   [1+1+1+3]
   (b) Why is bus arbitration required. Discuss about any two bus arbitration methods. [10]

3. (a) What is pipeline? Give the detailed picture of pipeline.
   (b) Explain pipeline for floating point addition and subtraction. [8+8]

4. (a) Explain Booth's algorithm with its theoretical basis.
   (b) Represent two n-bit unsigned numbers multiplications with a series of n/2-bit multiplications. [8+8]

5. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those.
   (b) Explain time-shared common bus Organization.
   (c) Explain system bus structure for multiprocessors [6+5+5]

6. Explain about instruction, fetch, and decode cycles for a memory reference instruction. Draw a flow chart also to explain the same. Indicate clearly where and which processor registers comes into picture. Now let us assume while a instruction is in the middle of its decode cycle a interrupt is arrived. What is going to happen? Is the instruction completed or not. If we want to stop there itself and handle the interrupt what are the difficulties? [16]

7. Explain the working of the following:
   (a) Page table

(b) TLB

(c) Memory Management Unit [5+5+6]

8. Explain the following:

(a) Peripheral Component Interconnect Bus (PCI)

(b) Universal Serial Bus (USB) [8+8]

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Code No: R05221901 **R05** **Set No. 1**

II B.Tech II Semester Examinations,April/May 2012
COMPUTER ORGANISATION
Common to Instrumentation And Control Engineering, Electronics And Computer Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the working of the following:
   (a) Page table
   (b) TLB
   (c) Memory Management Unit [5+5+6]
2. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those.
   (b) Explain time-shared common bus Organization.
   (c) Explain system bus structure for multiprocessors [6+5+5]
3. (a) Why do we need subroutine register in a control unit? Explain.
   (b) Explain nanoinstructions and nanometry. Why do we need them? [8+8]
4. (a) Find out what are the actual values of the following IEEE 754 single precision number.
      i. Sign=0, exponent=all 1s and fraction field is not 0.
      ii. Sign=0, exponent=all 0s and fraction field is 0.
      iii. Sign=1, exponent=all 1s and fraction field is 0.
      iv. Sign=0, exponent=1000 0001, fraction=1100 0000 0000 0000 0000 000

      [1+1+1+3]
   (b) Why is bus arbitration required. Discuss about any two bus arbitration methods. [10]
5. Explain the following:
   (a) Peripheral Component Interconnect Bus (PCI)
   (b) Universal Serial Bus (USB) [8+8]
6. (a) Explain Booth's algorithm with its theoretical basis.
   (b) Represent two n-bit unsigned numbers multiplications with a series of n/2-bit multiplications. [8+8]

7. Explain about instruction, fetch, and decode cycles for a memory reference instruction. Draw a flow chart also to explain the same. Indicate clearly where and which processor registers comes into picture. Now let us assume while a instruction is in the middle of its decode cycle a interrupt is arrived. What is going to happen? Is the instruction completed or not. If we want to stop there itself and handle the interrupt what are the difficulties? [16]

8. (a) What is pipeline? Give the detailed picture of pipeline.
   (b) Explain pipeline for floating point addition and subtraction. [8+8]

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Code No: R05221901 **R05** **Set No. 3**

II B.Tech II Semester Examinations,April/May 2012
COMPUTER ORGANISATION
Common to Instrumentation And Control Engineering, Electronics And Computer Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the following:
   (a) Peripheral Component Interconnect Bus (PCI)
   (b) Universal Serial Bus (USB) [8+8]
2. Explain the working of the following:
   (a) Page table
   (b) TLB
   (c) Memory Management Unit [5+5+6]
3. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those.
   (b) Explain time-shared common bus Organization.
   (c) Explain system bus structure for multiprocessors [6+5+5]
4. (a) Explain Booth's algorithm with its theoretical basis.
   (b) Represent two n-bit unsigned numbers multiplications with a series of n/2-bit multiplications. [8+8]
5. (a) Why do we need subroutine register in a control unit? Explain.
   (b) Explain nanoinstructions and nanometry. Why do we need them? [8+8]
6. (a) What is pipeline? Give the detailed picture of pipeline.
   (b) Explain pipeline for floating point addition and subtraction. [8+8]
7. (a) Find out what are the actual values of the following IEEE 754 single precision number.
      i. Sign=0, exponent=all 1s and fraction field is not 0.
      ii. Sign=0, exponent=all 0s and fraction field is 0.
      iii. Sign=1, exponent=all 1s and fraction field is 0.
      iv. Sign=0, exponent=1000 0001, fraction=1100 0000 0000 0000 0000 000

      [1+1+1+3]
   (b) Why is bus arbitration required. Discuss about any two bus arbitration methods. [10]

8. Explain about instruction, fetch, and decode cycles for a memory reference instruction. Draw a flow chart also to explain the same. Indicate clearly where and which processor registers comes into picture. Now let us assume while a instruction is in the middle of its decode cycle a interrupt is arrived. What is going to happen? Is the instruction completed or not. If we want to stop there itself and handle the interrupt what are the difficulties? [16]

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