Code No: R09220403 | R09 | SET-1

B.Tech II Year - II Semester Examinations, April-May, 2012
PULSE AND DIGITAL CIRCUITS
(Common to BME, ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Explain perfect compensation, over compensation and under compensation with respect to attenuator circuits?
b) Explain why the initial voltage distribution in an attenuator is determined by the capacitors?
c) Explain why the final voltage distribution in an attenuator is determined by the resistors?
d) Why does a resistive attenuator need to be compensated? [6+3+3+3]

2.a) The ideal transfer characteristic of particular clipper circuit is shown in Figure.1. Design the circuit using ideal diodes and draw the input-output waveforms with proper explanation, if $V_i = 10 \sin \omega t$.

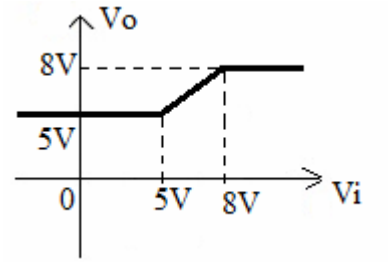

Figure.1

b) With neat diagrams, explain the use of clamper circuit in television receivers as DC restorer? [10+5]

3.a) Design a common-emitter transistor switch shown in Figure.2, operated with Vcc = 18V and -Vbb = -12V. The transistor is expected to operate at I_C = 8mA, I_B = 0.75mA. Assume h_{FE} =25, $V_{BE}(sat) = V_{CE}(sat)$ = 0V and $R_2 = 6\ R_1$.

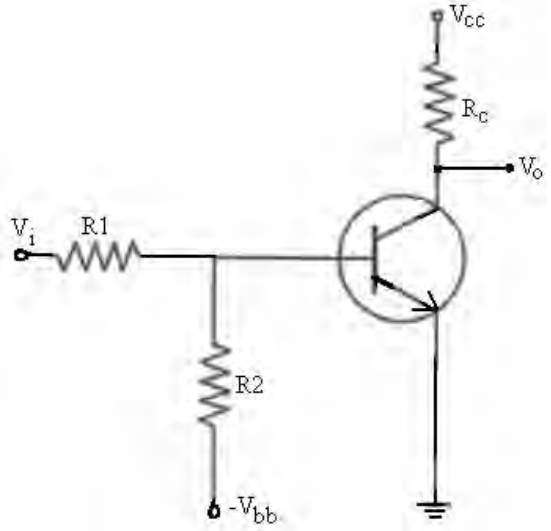

Figure.2

b) Define storage and transition times with respect to diodes? [12+3]

4. A self-biased binary uses n-p-n transistors have maximum values of $V_{CE}(sat)=0.4V$ and $V_{BE}(sat) = 0.8V$ and V_{BE} cutoff = 0V. The circuit parameters are $V_{CC} = 15V$, $R_C = 1K\Omega$, $R_1 = 6K\Omega$, $R_2 = 15K\Omega$ and $R_E = 500\Omega$.
a) Find the stable-state currents and voltages.
b) Find the minimum value of h_{FE} required for BJT to provide the above stable state values.
c) Also determine $I_{CBO}(max)$ to which I_{CBO} raises as temperature rises where neither BJT is off. [15]

5.a) Draw the circuit of simple current time-base generator and explain its operation with the help of neat waveforms and necessary equations. Also derive expression for sweep speed error(e_s), by considering the effect of internal resistance of inductor (R_L) and collector saturation resistance (R_{CS}) of the transistor.
b) Explain why an operational integrator is used in transistorized Miller sweep circuit? [12+3]

6.a) Draw and explain the circuit diagram of a six-diode sampling gate. Derive expressions for V_{Cmin}
b) For the four diode gate with a divider resistance $R=100\Omega$, $V_S=25V$, $R_f = 20$, $R_L = R_C = 200K\Omega$. Find V_{Cmin} and V_{nmin}? [10+5]

7.a) What type of synchronization is used when the interval between pulses is less than or equal to the natural period of the wave form generator? Explain it briefly.
b) With the help of neat diagram and wave forms explain the use of a monostable relaxation circuit as a frequency divider? [7+8]

8.a) Draw the circuit of a 2-input TTL totem-pole output NAND gate with the help of four transistors. Explain why the output of this gate cannot be wire-ANDed?
b) Explain the function of multi emitter transistor used in the above circuit. What is the disadvantage of using back to back diodes in place of multi emitter transistor?
c) Explain why this logic circuit is faster than open collector logic circuit?
[6+6+3]

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Code No: R09220403 | R09 | SET-2

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Time: 3 hours **Max. Marks: 75**

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1.a) Obtain an expression for the input impedance of RC differentiating circuit. Compare it with that of RL differentiating circuit.

b) A pulse of 5V amplitude and width of 0.5 msec. is applied to high pass RC circuit consisting of R = 22 KΩ and C = 0.47μF. Estimate the output voltage levels and sketch the waveform. Also determine the percentage tilt in the output? [5+10]

2.a) A voltage signal of 10 sin ωt is applied to the circuit with ideal diodes shown in Figure.1. Estimate the maximum & minimum values of output waveform and maximum current through each diode. Also draw the input-output waveforms with proper explanation.

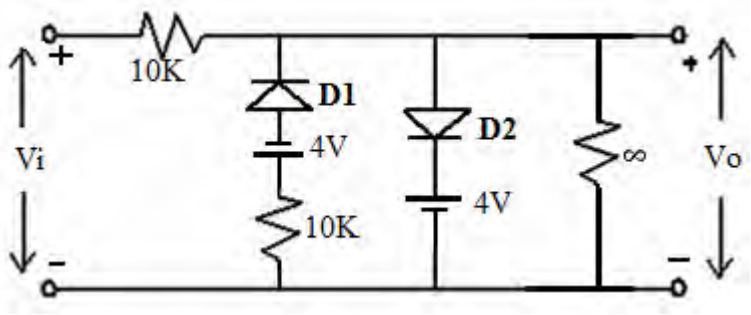

Figure.1

b) A square wave input is applied to the clamper circuit shown in Figure.2. By taking the effect of source resistance, R_s, the diode forward dynamic resistance, R_f and the diode reverse dynamic resistance, R_r into account, draw the equivalent circuits for the following cases:
i) When the diode is conducting ii) When the diode is not conducting. [9+6]

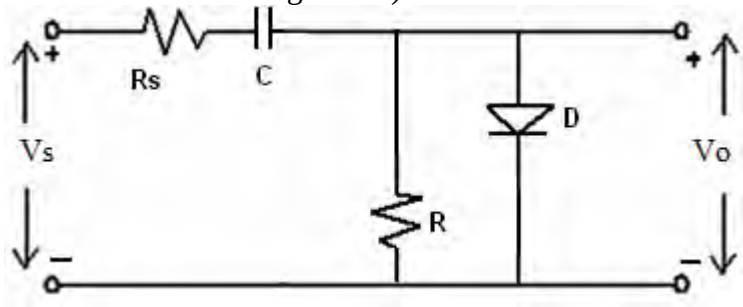

Figure.2

3.a) A simple diode-switch circuit and the input signal applied to it are shown in Figure.3. Draw and explain the waveforms representing the variation in minority carrier concentration, diode current I, and diode voltage$V_{D,}$ with respect to input signal variations.

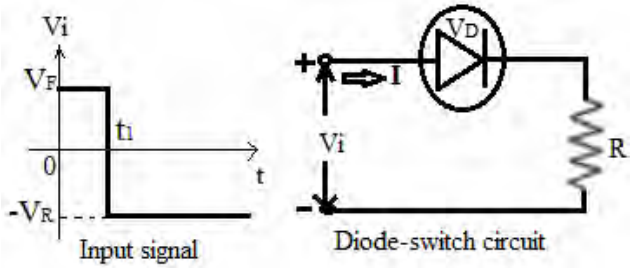

Figure.3

b) Derive an expression for collector-to-emitter breakdown voltage, with open-circuited base, BV_{CEO} in terms of collector-to-base breakdown voltage, with open-circuited emitter, $BV_{CBO.}$ [8+7]

4. What for the circuit shown in Figure.4 is used? Discuss the role of the diodes, D1 and D2 in the circuit. With neat waveforms and necessary equations, explain the operation of the circuit, without D1, D2, R3 and $R3^1$. [15]

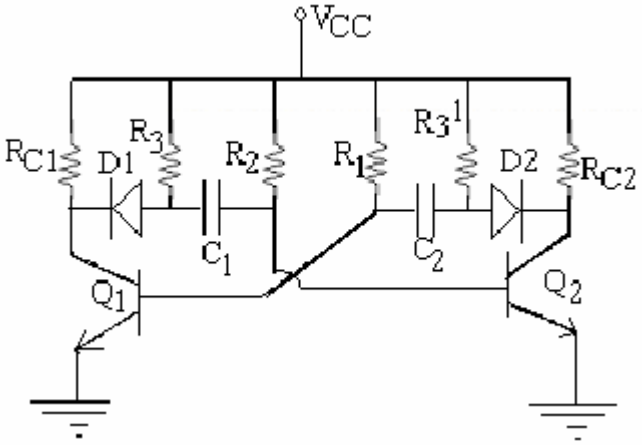

Figure.4

5.a) Draw and explain the operation of transistorized Miller sweep generator. Show that the sweep speed for Miller circuits is same as in the case where the capacitor, C charges through a resistor, R directly from the source, V.

b) A transistor bootstrap ramp generator is to produce a 15V, 5ms output to a 2KΩ load resistor. The ramp is to be linear within 2%. Design a suitable circuit using Vcc = 22V, -VEE = -22V and transistor with $h_{fe(min)}$ = 25, h_{ie} = 1.1KΩ, $h_{re}=2.5x10^{-4}$, h_{oe} = 25μA/V, $V_{BE(sat)}$ = 0.8V, $V_{BE(active)}$ = 0.7V, $V_{CE(sat)}$ = 0.2V. The input pulse has an amplitude of -5V, pulse width = 5ms and space width = 2.5ms. [7+8]

6.a) Explain how to cancel the pedestal in a sampling gate with suitable circuit diagram.

b) Explain the function of a sampling gate is used in Sampling Scopes. [7+8]

7.a) Explain the factors which influence the stability of a relaxation divider with the help of a neat waveforms.

b) A UJT sweep operates with valley voltage (V_v) = 3V, peak voltage (V_p) =16V and η = 0.5. A sinusoidal synchronizing voltage of 2V peak is applied between bases and the natural frequency of the sweep is 1 KHz, over what range of sync signal frequency will the sweep remain in 1:1 synchronism with the sync signal? [7+8]

8.a) With the help of circuit diagram explain the purpose of clamping diode in a positive diode AND gate.

b) What is meant by active pull-up? Draw the circuit of TTL active pull-up NAND gate and explain its operation with the help of function table? [7+8]

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Time: 3 hours **Max. Marks: 75**

Answer any five questions
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1.a) Which linear circuit is required to obtain the output for the given input shown in Figure.1. Explain its operation with necessary equations?

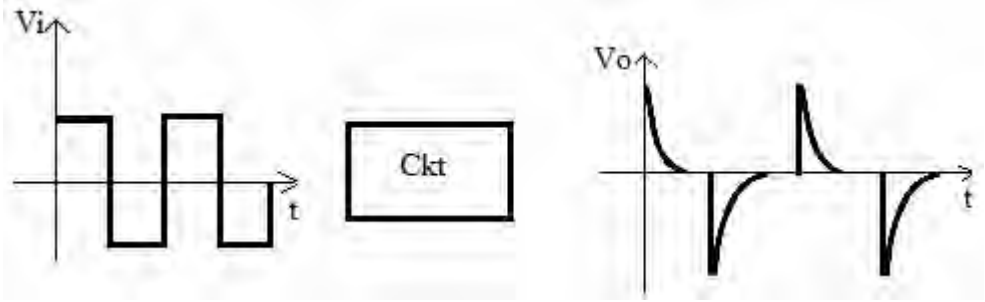

Figure.1

b) A constant voltage of 100V is applied to a series RLC circuit with L=10H, R=20Ω and C=5F. The initial current in the circuit is zero but there is an initial voltage of 50V on the capacitor in a direction which opposes the applied source. Find the expression for the current in the circuit and derive the expressions used. [7+8]

2.a) The ideal transfer characteristic of particular clipper circuit is shown in Figure.2. Design the circuit using ideal diodes and draw the input-output waveforms with proper explanation, if V_i = 15 Sin ωt.

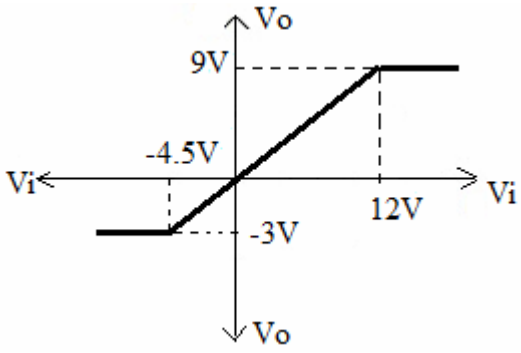

Figure.2

b) With neat diagrams, explain the use of clamper circuit in television receivers as DC restorer? [10+5]

3.a) With neat sketches and necessary expressions, explain the affect of temperature on the saturated junction voltages of a transistor.

b) For a CE transistor circuit shown in Figure.3, V_{CC} = 15V, R_C= 1.5K and I_B = 0.3mA. Determine the minimum value of h_{FE} required for saturation to occur. [7+8]

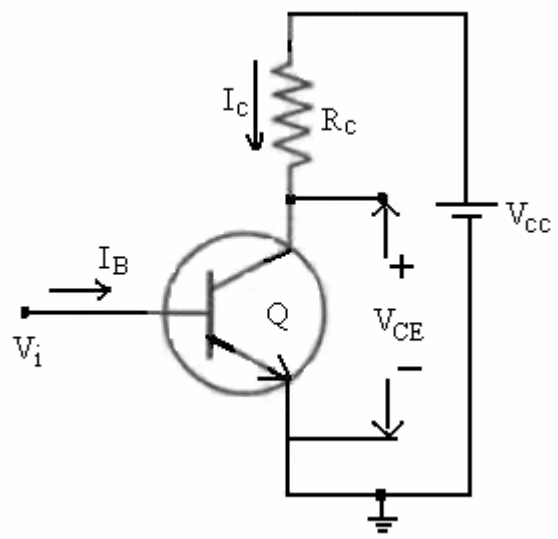

Figure.3

4.a) What are transpose capacitors? Explain how the commutating capacitors will increase the speed of a fixed-bias binary.

b) Design and draw a collector-coupled ONE-SHOT using silicon npn transistors with h_{FE}(min) =20. In stable state, the transistor in cut-off has V_{BE} = -1V and the transistor in saturation has base current, I_B which is 50% excess of the I_B(min) value. Assume V_{CC} = 8V, I_C(sat) =2mA, delay time = 2.5ms & $R_1 = R_2$. Find R_C, R, R_1, C and V_{BB}. [3+12]

5.a) Draw and explain the circuit of transistorized Bootstrap sweep generator. Derive an expression for retrace interval, T_r.

b) A transistorized Miller sweep generator has the following parameters: R=1.2MΩ, R_2 = 15 MΩ, R_3 = 120 KΩ, R_4 = 27 KΩ, R_5 = 100 KΩ and V_{BB} = 40V. The transistor h-parameters are h_{fe} = 50, h_{ie} = 1.1KΩ, $h_{re} = 2.5x10^{-4}$ and h_{oe} = 25μA/V. If the output sweep amplitude is 25V, find the slope error? [7+8]

6.a) Explain how the loading of the control signal is reduced when the number of inputs increases in a sampling gate?

b) Draw the circuit diagram of a unidirectional sampling gate which delivers an output only at the coincidence of a number of control voltages and explain its working. [7+8]

7.a) With the help of a circuit diagram and waveforms, explain how frequency division is done by an astable multivibrator?

b) Draw and explain the block diagram of frequency divider without phase jitter. [8+7]

8.a) Which is the fastest non-saturated logic family? With a neat circuit diagram explain its operation in view of logic of operation, noise margin, propagation delay and fan-out.

b) In 4-input NAND gate, two inputs are to be used. What are the options available for the unused inputs and which one is the best and why? [10+5]

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Code No: R09220403 | R09 | SET-4

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Time: 3 hours **Max. Marks: 75**

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1.a) An inductor does not allow sudden changes in current and a capacitor does not allow sudden changes in voltage. Justify with relevant equations.

b) What are the disadvantages of RL linear wave shaping circuit compared to RC circuit?

c) A symmetrical square wave of $\pm$ 5V at a frequency of 5 KHz is applied to a high pass RC circuit with a cut-off frequency of 20 KHz. Sketch the steady state input and output voltage waveforms. Calculate the steady state output voltage levels? [4+3+8]

2.a) A voltage signal of 10 sin ωt is applied to the circuit with ideal diodes shown in Figure.1. Estimate the maximum & minimum values of output waveform and maximum current through each diode. Also draw the input-output waveforms with proper explanation.

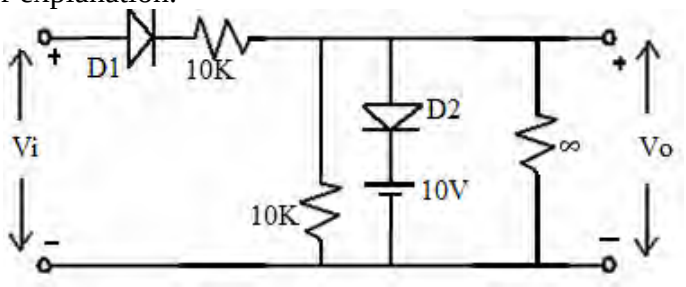

Figure.1

b) Explain the steps to analyze a clamping network with an example? [10+5]

3.a) Calculate the output levels of the circuit shown in Figure.2, for the inputs 0 and -6 Volts and verify that the circuit is an inverter. What is the minimum value of h_{FE} required? Neglect junction saturation voltages and assume an ideal diode.

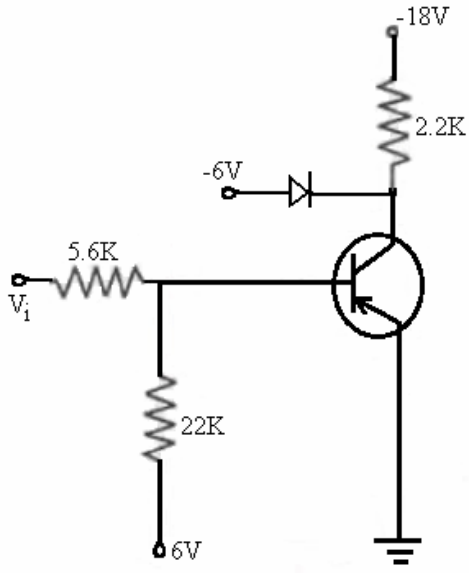

Figure.2

b) With neat sketches representing minority-carrier density distribution as a function of distance from junction, explain the diode reverse recovery time in detail? [10+5]

4.a) Explain various methods to improve the resolution of a binary.

b) Design a Schmitt trigger circuit using npn silicon transistors with V_{BE} = 0.7V, $V_{CE(sat)}$ = 0.2V, h_{fe}(min) = 60 and $I_{C(ON)}$ = 3mA to meet the following specifications: V_{CC} =12V, upper threshold voltage, V_{UT} = 4V, lower threshold voltage, V_{LT} =2V. [3+12]

5.a) Prove that when restoration time is zero, saw-tooth output waveform can be obtained from a sweep generator circuit.

b) The transistorized Bootstrap sweep generator circuit has the following parameters: V_{CC} = 25V, $-V_{EE}$ = -15V, R = 10 KΩ, R_B = 150 KΩ, R_E= 1KΩ, C = 0.05 µF. The gating waveform has 300µs duration. The transistor parameters are h_{ie} = 1.1KΩ, h_{re} = 2.5 x 10^{-4}, h_{fe} =50, h_{oe} = 25µA/V.
i) Draw the waveforms for the collector current of input transistor (Q_1), I_{C1} and output voltage at the emitter of output transistor (Q_2), labeling all current and voltage levels?
ii) What is the slope error of the sweep?
iii) What is the sweep speed and the maximum value of the sweep voltage?
iv) What is the retrace time T_r for C to discharge completely?
v) Calculate the recovery time T_1 for C_1 to recharge completely? [7+8]

6.a) Draw the bidirectional diode sampling gate in the form of a bridge network and explain its working.

b) Explain how a sampling gate is used in chopper amplifier? [8+7]

7.a) What do you mean by synchronization ?

b) What is the condition to be met for pulse synchronization?

c) Compare sine wave synchronization with pulse synchronization? [3+6+6]

8.a) Compare the RTL and DTL logic families in terms of Fan out, propagation delay, power dissipated per gate and noise immunity.

b) What is meant by tri-state logic? Draw the circuit of tri-state TTL logic and explain its operation in detail? [8+7]

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