

B.Tech II Year - II Semester Examinations, April-May, 2012
COMPUTER ORGANIZATION AND ARCHITECTURE
(Electronics and Computer Engineering)

Time: 3 hours

Max. Marks: 75

Answer any five questions
All questions carry equal marks

- - -

- 1.a) What is System Software? What are the functions performed by Software?
 b) Evaluate $(-638) + (+785)$ using the signed 10's complement representation for negative numbers. [15]
- 2.a) Design a 4 bit combinational circuit decremter using four full adder circuits.
 b) Write a short note on Register transfer language. [15]
- 3.a) Write a program to evaluate the arithmetic statement

$$X = \frac{A - B + C * (D * E - F)}{G + H * K}$$
 using a general register computer with two address instructions.
 b) Write short notes on Stack Organization. [15]
- 4.a) What is mapping process? How is an instruction mapped?
 b) Explain the differences between micro code and micro operation. [15]
- 5.a) What is the function of cache memory? Explain the terms cache hit and cache miss.
 b) An address space is specified by 24 bits and the correspond memory space by 16 bits.
 i) How many words are there in the address space?
 ii) How many words are there in the memory space?
 iii) If a page consists of 2K words, how many pages and blocks are there in the system? [15]
- 6.a) Discuss RS 232C standards for serial data transfer.
 b) Write short notes on CPU-IOP communication. [15]
7. What are the several ways in which branch instructions can be handled in order to avoid performance degradation caused by instruction branching. Explain them with examples. [15]
- 8.a) Write short notes on
 i) Hardware lock ii) Sema – phore.
 b) How can the problem of cache wherence be resolved with a snoopy cache controller? [15]

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- 1.a) What are the functional units of a computer? Explain.
- b) How is the performance of a computer determined?
- c) Perform the arithmetic operation $(+42) + (-13)$ in binary using signed 2's complement of the subtrahend. [15]

- 2.a) What is the difference between logical shift and circular shift left? Explain with examples.
- b) Design a bus system for 4 registers using multiplexers. [15]

- 3.a) Write a program to evaluate the arithmetic statement

$$X = \frac{A - B + C * (D * E - F)}{G + H * K}$$
 using a general register computer with three address instructions.
- b) Explain the sequence of events in an interrupt cycle. [15]

- 4.a) Explain the difference between hardwired control and micro programmed control.
- b) What are the functional parts of a micro instruction format? Explain. [15]

- 5.a) What is a memory controller? For what type of Semi conductor memory is it used. What are its functions?
- b) The access time of a cache memory is 100 ns and that of main memory 1000 ns. It is estimated that 80% of the memory requests are for read and the remaining 20% for write. The hit ratio for read access only is 0.9. A write through procedure is used.
 - i) What is the average access time of the system considering only memory read cycles?
 - ii) What is the average access time of the system for both read and write requests?
 - iii) What is the hit ratio taking into consideration the write cycles? [15]

- 6.a) Write short notes on Universal Serial BUS.
- b) What is the difference between a subroutine and an interrupt service routine? [15]

- 7.a) Formulate a four – segment instruction pipeline for a computer. Specify the operations to be performed in each segment.
- b) Give an example of a program that will cause data conflict in a three segment pipeline. [15]

- 8.a) What are the different dynamic arbitration algorithms? Explain any two.
- b) Explain the write – through and write – block protocols. [15]

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- 1.a) What is a bus? Explain the single bus structure.
- b) Write short notes on
 - i) Compiler
 - ii) Operating System. [15]
- 2.a) Design a 4 – bit combinational circuit shifter with two select lines for shift right and shift left.
- b) What are the different arithmetic micro operations? Explain with examples. [15]
- 3.a) A first – in, first – out (FIFO) has a memory organization that stores information in such a manner that the item that is stored first is the first item that is retrieved. Show how a FIFO memory operates with three counters.
- b) Convert the following numerical arithmetic expression into reverse polish notation.

$$(3+4)[10(2+6)+8]$$
 [15]
- 4.a) What is the function of control memory? What is the address sequencing capabilities required in a control memory?
- b) How can branch logic hardware be implemented? [15]
- 5.a) Discuss real and virtual memory. What is logical address and physical address?
- b) A two – way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128K×32.
 - i) Formulate all pertinent information required to construct the cache memory.
 - ii) What is the size of the cache memory? [15]
- 6.a) Explain
 - i) Simplex
 - ii) half – duplex
 - iii) full duplex modes.
- b) Explain the working of a daisy chain priority interrupt. [15]
- 7.a) What is a hazard? What are the different kinds of hazards encountered during execution of a pipeline?
- b) Determine the number of clock cycles that it takes to process 200 tasks in a Six – Segment pipeline. [15]
- 8.a) Explain how a cross bar inter connection network works.
- b) What is cache coherence and explain its importance in shared memory multiprocessor systems? [15]

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- 1.a) What are the various computer types? Explain.
- b) Explain the usage of buffer register. [15]

- 2.a) What is the difference between logical shift right and arithmetic shift right? Explain with examples.
- b) Explain the various phases in an instruction cycle. [15]

3. Write a program that can evaluate the expression
 $A*B+C*D$
in a single accumulator processor. Assume that the processor has load, store, multiply and Add instructions. [15]

- 4.a) What are the steps that the control must under go during the execution of a single instruction?
- b) Explain the usage of a control address register. [15]

- 5.a) What are the different types of magnetic memory? Describe them briefly.
- b) A digital computer has a memory unit of $64K \times 16$ and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.
 - i) How many bits are there in a tag, index, block and word fields of the address format?
 - ii) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.
 - iii) How many blocks can the cache accommodate? [15]

- 6.a) Explain IEEE 1394 standard for high-speed serial data transfer.
- b) Write short notes on hand shaking. [15]

- 7.a) What is an array processor? What are the different types of array processors?
- b) Draw a space-time diagram for a four – segment pipeline showing the time it takes to process six tasks. [15]

- 8.a) How does a hyper cube inter connection work?
- b) Differentiate between serial arbitration logic and parallel arbitration logic. [15]
