Code No: 07A3EC16 **R07**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year I Semester Examinations, November/December-2013
Digital Logic Design
(Common to CSE, IT)

Time: 3 hours **Max. Marks: 80**

Answer any five questions
All questions carry equal marks
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1.a) Convert the following numbers to hexadecimal.
i) $(360)_8$ ii) $(37.29)_{10}$ iii) $(11100.1101)_2$ iv) $(789)_{10}$
b) Explain about complement representation and also explain 2's complement with example. [8+8]

2.a) Explain the demorgan's theorems in Boolean algebra.
b) List and prove the fundamental postulates of Boolean algebra. [8+8]

3.a) Find the reduced POS form of the following equation and also implement using NAND logic.
$$F(A, B, C) = \sum m(1, 3, 7, 11, 15) + \sum d(0, 2, 5)$$
b) What are the limitations of karnaugh map(K-map). [10+6]

4.a) Implement the following Boolean function using 4:1 Mux
$$F(P, Q, R, S) = \sum m(0, 1, 3, 4, 8, 9, 15).$$
b) Give the schematic circuit of a 2 to 4 Binary Decoder with an active – low enable input. Give the truth table for the same. [8+8]

5.a) Compare combinational Vs sequential logic circuits with suitable examples.
b) Give the transition table for the following flip-flop. [8+8]
i) RS flip-flop ii) JK flip-flop iii) D flip-flop iv) T flip-flop.

6. Explain the following with neat diagrams.
a) Serial addition in 4-bit shift register.
b) Universal Shift Register. [8+8]

7.a) Design a BCD to Excess-3 code converter using suitable PLA.
b) Compare PROM, PLA and PAL. [10+6]

8.a) Explain asynchronous sequential logic circuits with latches.
b) Write a Short note on races, cycles and hazards. [8+8]

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