R09

Code No: 09A30503

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year I Semester Examinations, November/December-2013
Digital Logic Design
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Convert the following numbers
i) $(10101100111.0101)_2 = (\ )_{10}$
ii) $(153.513)_8 = (\ )_{10}$
b) Perform the subtraction of the given binary numbers using 2's complement
i) 110110-100111
ii) 1011.11-101.001 [15]

2. Convert the following expression to Sum of Product form
a) (A'+B+C) (A+B'+C') (ABC)
b) (A+B+C') (A'+B'+C') (A'+B+C) [15]

3. Using Map method simplify the following expression and implement Logic circuit after minimization F(P, Q, R, S) = $\sum$m (0, 1, 4, 8, 9, 10) + d(2, 11). [15]

4.a) Explain the working of 2-bit magnitude comparator.
b) Draw the logic diagram of 4×1 multiplexer and explain its working. [15]

5.a) What is the difference between latch and flip flop? Explain the working of clocked RS flip flop with a diagram.
b) Explain working of JK Master Slave flip flop. [15]

6.a) Explain the working of Mod-10 ripple counter.
b) Explain the working of serial-in parallel-out shift register with a diagram. [15]

7.a) Explain different types of memory. Explain Error detection and error correction of ROM.
b) Write short notes on programmable array logic. [15]

8.a) Write a procedure for analysing an asynchronous sequential circuit with SR latch.
b) Write about Hazards in sequential circuits. [15]

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