Code No: 09A40204 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year II Semester Examinations, November/December-2013
SWITCHING THEORY AND LOGIC DESIGN
(Common to EEE, ECE, BME, ETM)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) List out the difference between weighted codes and non weighted code.
b) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.
i) 10010 and 10000.
ii) 1001100 and 1011100. [7+8]

2.a) State and prove postulates and theorems of Boolean algebra.
b) Draw the logic diagram and list the truth table of the given function.
F = xy + xy' + y'z [7+8]

3.a) Minimize the following Boolean function using K-map.
F = Π (2, 7, 8, 9, 10, 12).
b) Use Tabulation method and simplify the following function.
$f = \sum(2, 3, 5, 6, 7, 9, 12, 14, 15)$ [8+7]

4.a) What is decoder? Construct 3×8 decoder using logic gates and truth table.
b) Implement full adder using decoder and OR gates. [8+7]

5.a) Generate a PLA program table to design a BCD to excess-3 code converter.
b) Write a brief note on multi gate synthesis of threshold logic. [7+8]

6.a) Give the design of 4 bit Ring counter and explain its operation with waveforms. Also give the applications of ring counter.
b) Design a modulo-9 counter using T flip flops with preset and clear inputs. [7+8]

7. Find the equivalence partition for the machine shown below. Show a standard form of the corresponding reduced machine. [15]

PS	NS, Z	
	X=0	X=1
A	E,0	C,0
B	C,0	A,0
C	B,0	G,0
D	G,0	A,0
E	F,1	B,0
F	E,0	D,0
G	D,0	G,0

8. Design the ASM chart, data path circuit, control circuit using multiplexers for weighing machine. [15]

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