Code No: 09A60502 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B. Tech III Year II Semester Examinations, November/December-2013
VLSI DESIGN
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Discuss fabrication differences between NMOS and CMOS technologies. Which fabrication is preferred and why?
b) Explain about Ion Implantation process of IC Fabrication. [8+7]

2.a) Derive the relation between I_{DS} and V_{DS} of a MOSFET.
b) Draw the circuit for NMOS inverter and explain its operation. [8+7]

3.a) What is a stick diagram? Draw the stick diagram and layout for a CMOS inverter.
b) What are the effects of scaling on Vt?
c) What are design rules? Why is metal-metal spacing larger than poly-poly spacing. [5+5+5]

4.a) Draw the CMOS circuit to realize the Boolean expression y = A-B, and explain the same.
b) What is meant by fan-in and fan-out of a gate? [8+7]

5.a) Draw and explain the layout for a combinational adder appropriate for a datapath.
b) Draw the serial/parallel multiplier structure and explain how multiplication is performed. [8+7]

6.a) Draw the circuit for 4 transistor SRAM and explain its working.
b) Draw the one cell dynamic RAM circuit and explain its working. [8+7]

7.a) Draw and explain the FPGA chip architecture.
b) Draw and explain the AND/OR representation of PLA. [8+7]

8.a) Why chip testing is needed? At what levels testing a chip can occur?
b) Explain about system level test techniques. [8+7]

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