R09

Code No: 54021

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year II Semester Examinations, December-2014/January-2015
PULSE AND DIGITAL CIRCUITS
(Common to ECE, BME, ETM)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) A Symmetrical square wave of peak-to-peak amplitude 'V' and frequency 'f' is applied to a RC High pass circuit. Show that the fractional tilt is given by $P = \prod f_1/f$. Where f_1 is the lower 3dB frequency of RC High pass circuit.

b) RC Low pass circuit with R = 40 k ohms, C = 0.2μf is given a square wave input of 20V peak and 10msec period. What will be the amplitude be of settled output voltage wave form?

2.a) Design and draw a diode clipper circuit to clip the given input voltage of 10sinwt at +3Vand -5V level. Sketch the waveforms neatly.

b) State and prove clamping circuit theorem.

3.a) Explain in detail about piece-wise linear diode characteristics.

b) Discuss in detail about breakdown voltages of a transistor.

4.a) Derive an expression for gate width of a monostable multivibrator.

b) With the help of a neat circuit diagram, explain the operation of a astable multivibrator.

5.a) Explain briefly about different methods of generating time-base waveform.

b) Discuss in detail about correction of linearity through the adjustment of driving waveform for a current time-base waveform.

6.a) With the help of a neat circuit diagram and waveforms, explain the frequency division by astable blocking oscillator.

b) With the help of neat waveforms, explain sine wave frequency division with a sweep circuit.

7.a) With the help of a neat circuit diagram and waveforms, explain the operation of unidirectional diode sampling gate to accommodate more than one input signal.

b) Explain in detail about one application of sampling gates.

8.a) With the help of neat circuit diagram and truth table explain:
i) DL AND gate ii) RTL AND gate.

b) With the help of neat circuit diagram and truth table explain:
i) CMOS NAND gate ii) TTL NAND gate.

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