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R09

Code No: 57035

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech IV Year I Semester Examinations, December - 2014

VLSI DESIGN

(Common to ECE, EIE, BME, IT, ECM, ICE)

Time: 3 Hours

Max. Marks: 75

Answer any Five Questions

All Questions Carry Equal Marks

- 1.a) Write a note on microelectronics evolution.
- b) Write the comparisons between nMOS and Bipolar technologies.
- c) With a neat sketch explain CMOS fabrication in detail.

- 2.a) Derive the relationship between I_{DS} versus V_{DS} for a MOS transistor.
- b) Describe the operation of a pass transistor.

- 3.a) Explain the $2\mu m$ CMOS design rules in detail.
- b) List and explain the scaling factors for device parameters briefly.

- 4.a) What are the issues that happen when large capacitive loads are to be driven?
How to overcome them?
- b) Implement two input EX-NOR gate by using transmission gates.

- 5.a) Explain the operation of 4×4 Barrel Shifter with its circuit diagram.
- b) Design a 4 bit Comparator which gives outputs $A=B$, $A>B$ and $A<B$.

- 6.a) Explain the operation of control addressable memory.
- b) Explain about Serial access memories.

- 7.a) Implement 3-bit synchronous counter using PAL.
- b) Describe about FPGA architecture in detail.

- 8.a) Explain the chip-level test techniques in detail.
- b) Write about layout Design for improved Testability.

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