Code No: 5157M

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech II Semester Examinations, October - 2015
CMOS MIXED SIGNAL CIRCUIT DESIGN
(VLSI System Design/VLSI Design)

Time: 3 Hours **Max. Marks: 60**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 8 marks and may have a, b, c as sub questions.

PART - A

5 × 4 marks = 20

1.a) Explain the Charge Injection Cancellation in Switched capacitor circuits with neat diagram. [4]
b) Explain the block diagram of PLL. [4]
c) Write short notes on Hybrid converters. [4]
d) What is Interpolating? Explain. [4]
e) What is the importance of oversampling converters? Explain. [4]

PART - B

5 × 8 marks = 40

2. Explain about Unity-Gain Sampler/Buffer with neat circuit diagram. [8]

OR

3. Discuss the non-ideal effects in switched capacitor circuits. [8]

4.a) Explain the dynamics of simple PLL.
b) Discuss about jitter in PLLs. [4+4]

OR

5. Explain in detail about charge-pump PLLs. [8]

6. List and explain the DC and Dynamic specifications of data converters. [8]

OR

7. Briefly discuss about binary scaled converters. [8]

8. Explain about Two-step A/D converters. [8]

OR

9. Explain about Folding A/D converters. [8]

10. Discuss in detail about higher order Modulators with respect to oversampling converters. [8]

OR

11. Explain in detail about Delta sigma D/A converter. [8]

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