JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech II Semester Examinations, April-2015
HARDWARE - SOFTWARE CO-DESIGN
(Embedded Systems)

Time: 3 Hours   Max. Marks: 60

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 8 marks and may have a, b, c as sub questions.

PART - A

5 × 4 marks = 20

1.a) Differentiate static and dynamic partitioning techniques.
   b) Write a note on Source level debugging.
   c) Explain the important non-functional constraints that has influence in embedded system design.
   d) Discuss the development needs of embedded software in codesign.
   e) Explain in brief the terms, Design and Co-design.

PART - B

5 × 8 marks = 40

2. Explain in detail the generic co design methodology.   [8]

OR

3. Explain in brief the following computational models used in system design:
   a) FSM   b) DFG   c) PSM.   [8]

4. Explain the different design flow integrations for emulation systems.   [8]

OR

5. Explain in detail Euclid's GCD algorithm with a neat flow graph, RT circuit and controller graph.   [8]

6. Draw the flow chart to show the traditional compilation process and discuss the major problems encountered when adapting traditional compilation model to embedded processors.   [8]

OR

7. Explain in detail the concepts of retargetability and compiler validation. [8]

8. Define Validation. Explain the host-based compiler validation strategy. [8]

OR

9. What is meant by verification? Discuss in detail the verification tools used in co-design.   [8]

10. Explain in detail the approaches for hardware validation and differentiate them. [8]

OR

11. What is Hardware Software partitioning? Explain the Lycos system.   [8]

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