Code No: 124AF

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, December - 2017

DIGITAL DESIGN USING VERILOG HDL

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a)	Explain about strobe tasks.	[2]
b)	Define logic levels relevant to verilog HDL.	[3]
c)	What is drive strength of a device or gate in verilog.	[2]
d)	Explain NOR gate primitive with example.	[3]
e)	Define fork-join block.	[2]
f)	Define force-release construct with an example.	[3]
g)	Design verilog module for 4-bit full adder using dataflow operators.	[2]
h)	What is recursive function	[3]
i)	Write a short note on design verification.	[2]
j)	Explain about implicit model.	[3]

PART- B

(50 Marks)

2.a)	Explain the synthesis procedure in verilog HDL.	
b)	Classify the data types and explain.	[5+5]
	OR	
3.a)	Explain different levels of design description in verilog.	
b)	What are the functions of programming language interface (PLI)? Explain.	[5+5]
4.a)	Write notes on tristate gates. Give the relevant syntax, logic diagrams and excitation tables.	
b)	Discuss about strings in detail.	[5+5]
	OR	
5.a)	Explain continous assignment structures with examples.	
b)	Write about net delay with an example.	[5+5]
6.a)	Design verilog module to identify the highest priority interrupts.	
b)	Write test bench simulation results of above question with explanation.	[5+5]
	OR	
7.a)	Write the differences between begin-end and fork-join blocks.	
b)	Explain about multiple always blocks.	[5+5]

8.a) What do you mean by user defined primitive? Explain the types with examples.
b) Explain briefly the module paths. [5+5]

OR

9.a) Discuss the basic transistor switches.
b) Explain the computer directives. [5+5]

10.a) Write and explain the verilog module for positive edge trigger flip-flop.
b) Discuss setup hold, width and period checks used in verilog. [5+5]

OR

11.a) Explain cross coupled NOR latch.
b) What are the various sequential memory storage models explain in detail. [5+5]

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