Code No: 5455AF

R17

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech I Semester Examinations, January - 2018
CPLD AND FPGA ARCHITECTURES AND APPLICATIONS
(Embedded Systems)

Time: 3hrs **Max.Marks:75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

5 × 5 Marks = 25

1.a) Distinguish between programmable logic devices. [5]
b) Discuss about the technology mapping for FPGAs. [5]
c) List out the salient features of Xilinx 3000 CLB. [5]
d) Explain about how anti-fuse programming technology used in Actel FPGAs. [5]
e) What are the general design issues of FPGAs in design applications? [5]

PART - B

5 × 10 Marks = 50

2. Explain the various architectures of Xilinx Cool Runner CPLDs. [10]

OR

3. What is meant by programmable logic device? Draw and explain the basic architectures of CPLD and FPGA. Give the salient features, applications of the same. [10]

4. With neat diagrams, explain logic block architectures of FPGAs. [10]

OR

5.a) What is an FPGA. Explain about "why Field Programmable Gate Arrays".
b) Explain one time programmable based FPGA? Explain its basic programming elements. [5+5]

6. Write about SRAM Programming technology of programmable FPGAs with neat sketches. [10]

OR

7. Draw the schematic diagram of Xilinx based XC4000 CLB and describes its functional operation. [10]

8. Discuss the architectural differences of Act1, Act2 family FPGAs. [10]

OR

9. Explain how Actel's ACT2 FPGA Family is architecturally close to MPGA with neat diagram. [10]

10. How would you implement a binary counter using the CLBs of FPGA? Explain. [10]

OR

11. Write short notes on
a) A position tracker for a Robot Manipulator
b) Designing counters with ACT. [5+5]

---ooOoo---