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Code No: 5455AX

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech II Semester Examinations, June/July - 2018
HARDWARE SOFTWARE CO-DESIGN
(Embedded Systems)

Time: 3hrs **Max.Marks:75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

5 × 5 Marks = 25

1.a) Explain FSM architecture. [5]
b) Explain the impact of component specialization techniques on target architectures. [5]
c) Distinguish various application system classes. [5]
d) Identify major hurdles a software tool designer encounters while adapting traditional compilation model to embedded processors. [5]
e) Write about system level specification languages. [5]

PART - B

5 × 10 Marks = 50

2. Discuss in detail Generic co-design methodology. [10]

OR

3. Explain at least one model for capturing the behavior of single and multi-rate Co-synthesis systems separately. [10]

4. Explain about Quick turn Emulation systems. [10]

OR

5. Discuss about the system communication infrastructure. [10]

6. Elucidate Mixed and less specialized class of target architectures. [10]

OR

7. Explain about different types of compilation technologies. [10]

8.a) Discuss tools necessary for embedded processor based designs.
b) Discuss co-design computation model and its design. [5+5]

OR

9. Define concurrency and discuss different situations the concurrency abstraction covers. [10]

10. Describe about LYCOS system. [10]

OR

11. Discuss System level heterogeneous specification schemes with supporting environment. [10]

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